ADM-PA100
User Manual

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1 Introduction

The ADM-PA100 is a high-performance reconfigurable computing card featuring the latest Xilinx Adaptive Compute Acceleration Platform (ACAP) platform known as Versal. The PCIe form factor is ideal for Data Center applications and general evaluation and deployment of this new architecture. The card features a full FMC+ interface, two banks of 72-bit DDR4-SDRAM, front panel Ethernet, PMOD, USB, and Samtec FireFly.

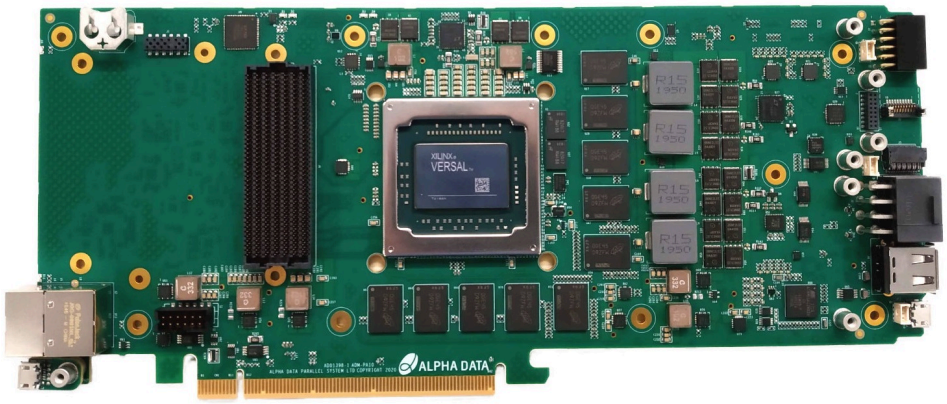

Figure 1 : ADM-PA100 Product Photo

1.1 Key Features

Key Features

- PCIe Gen3 x16 and dual Gen4x8 capable
- 2-slot active or passive heat sink
- 3/4 length, full profile, x16 edge PCIe form factor
- Supports Versal XCVC1902 ACAP devices in the VSVA2197 package
- FMC+ front panel interface:
  - 24 high speed serial channels capable of 32Gbps each
  - 160 single ended general purpose signals (80 differential pairs)
  - 1.5-1.0V VADJ voltage range
  - Extra clearance for optical cages
- Versatile MIO interface support:
  - GEM0 Ethernet access through RJ45 at front panel
  - 12 MIO GPIO accessible at rear
  - uSD
  - Dual QSPI
  - ULPI USB PHY accessible at USBA receptacle
  - 2x UART broken out through micro-USB at PCIe front panel and rear
- Two separate banks of 64 bit + ECC (72 bit total) DDR4-3200 SDRAM
- One internal FireFly site with 4 channels each capable of 28Gbps operation
- Front panel and rear edge JTAG access via USB port
- ACAP configurable over USB/JTAG and SPI configuration flash
- Voltage, current, and temperature monitoring
- Digilent PMOD 3.3V, 12-pin interface accessible to PL
- 2 user LEDs and 2 user switches

1.2 Order Code

See the PA100 datasheet for complete ordering options.

2 Board Information

2.1 Physical Specifications

The ADM-PA100 complies with PCI Express CEM revision 4.0.

Description	Measure
PCB Dy	111.15 mm
PCB Dx	254 mm
PCB Dz	1.6 mm
Circuit assembly weight	210 grams

Table 1 : Mechanical Dimensions (PCB only)

Description	Measure
Total Dy	126.3 mm
Total Dx	267.2 mm
Total Dz	39.9 mm
Total weight (with heat sink)	890 grams

Table 2 : Mechanical Dimensions (Fully Assembled)

Total weight does not include the PCIe Handle, which is optional and shipped uninstalled.

Figure 2 : ADM-PA100 Fully Assembled

2.2 Chassis Requirements

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2.2 PCI Express

The ADM-PA100 is capable of PCIe Gen 1/2/3 with 1/4/8/16 lanes, and PCIe Gen 4 with 1/4/8 lanes when using the Xilinx Integrated Block for PCI Express. PCIe Gen 4x8 can be bifurcated into two slots to achieve an aggregate bandwidth of a 16 lane connection.

2.2.3 Mechanical Requirements

A 16 lane physical PCIe slot is required for mechanical compatibility.

The card is also designed to use the extra mechanical retention mechanisms defined in the PCIe specification. This includes both the board keep out region along the top edge, and the full-length handle support. It is recommended to use all board retention features supported by the host systems. These cards are heavy and can be damaged when used in systems that do not mechanically support the hardware properly.

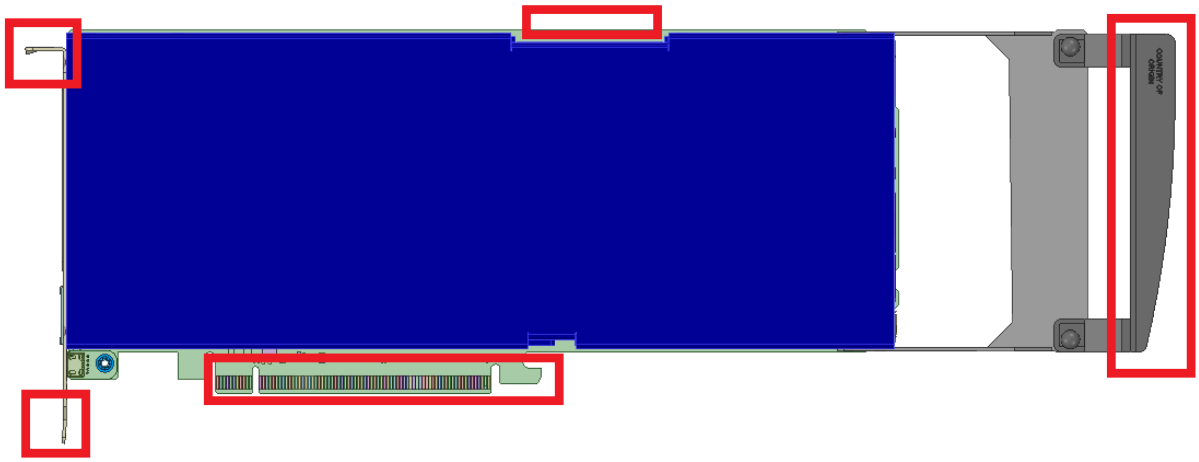

Figure 3 : Retention Points

2.2.4 Power Requirements

The ADM-PA100 draws power from the PCIe Edge and the 8-pin ATX power connector. The ADM-PA100 does not use or require the 3.3V power from the PCIe Edge (though it does use 3.3V AUX). To operate with PCIe edge only, ensure SW1-6 is OFF (see Switches). As per PCIe specification, users should limit the board power consumption to 66W when using only the PCIe edge power. Adding the 8-pin ATX connector provides additional 150W of power, bringing the total board power dissipation maximum to 216W.

It is possible to operate this product standalone with power from the 8-pin ATX power connector alone. Please be aware this reduces the total rated power of the card to 150W. Standalone operation requires a modified ATX power cable where the sense wires have been removed. Please contact **sales@alpha-data.com** to receive a modified ATX extension cable. When using a cable with the sense wires removed, ensure SW1-6 is set OFF which enables the 12V auto-detect feature. If SW1-6 is ON, the board will not power up unless both PCIe edge and the Aux cable are both used.

Power consumption estimation requires the use of the Xilinx XPE spreadsheet (www.xilinx.com/products/technology/power/xpe.html) and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.85-0.90	VCC_INT	150A
0.85-0.90	VCC_IO + VCC_PMC + VCC_PSFP + VCC_PSLP + VCC_RAM + VCC_SOC	10A
0.88	MGTAVCC	8A
1.2	MGTAVTT	8A
1.2	VCCO + DDR4	8A
1.5	GTY_AVCCAUX	2A
1.5	VCCO + VCCAUX + VCCAUX_PMC	8A
1.0-1.5	FMC_VADJ + VCCO	8A
3.3	VCCO + FMC+	8A

Table 3 : Available Power By Rail

2.3 Thermal Performance

If the ACAP core temperature exceeds 105 degrees Celsius, the ACAP design will be cleared to prevent the card from over-heating.

The ADM-PA100 comes with a heat sink to avoid thermal overstress of ACAP, since it is typically the hottest point on the card. The ACAP die temperature must remain under 100 degrees Celsius. To estimate the ACAP die temperature: first take your total board power (see next paragraph), then multiply by Theta JA from the graph below, and add the resulting temperature to your system internal ambient temperature. If you are using the fans provided with the board, you will find theta JA is approximately 0.3 degC/W for the board in still air.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the Xilinx Power Estimator (XPE) downloadable at www.xilinx.com/products/technology/power/xpe.html. Download the Versal tool and set the device according to your part number details: Versal AI Core Series, XCVC1902, VSVA2197 package, -2MS/-3HS speed grade, extended. Set the ambient temperature to your system ambient and select 'user override' for the effective theta JA. Then enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next acquire the PA100 power estimator from Alpha Data by contacting **support@alpha-data.com**. Enter in the power figures from XPE, FMC+ (if used), and DRAM utilization into the Alpha Data spreadsheet to get a complete board level estimate.

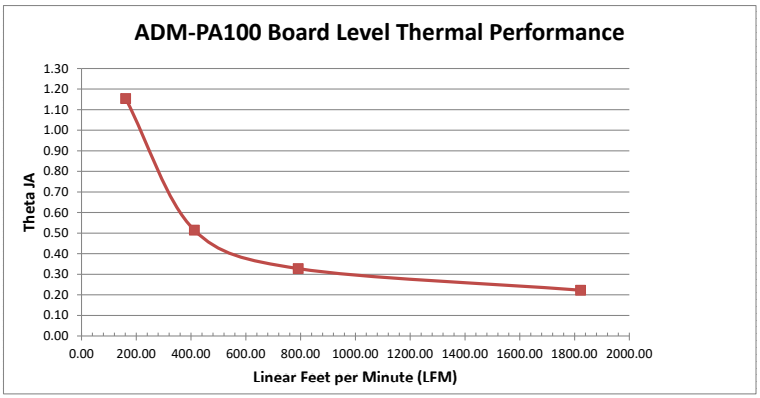

Figure 4 : Thermal Performance

2.4 Customizations

Alpha Data provides extensive customization options to existing commercial off-the-shelf (COTS) products. Some options include, but are not limited to: custom front panel interfaces, additional networking cages in adjacent slots, enhanced heat sinks, baffles, and circuit additions.

Please contact **sales@alpha-data.com** to get a quote and start your project today.

3 Functional Description

3.1 Overview

The ADM-PA100 is a high-performance reconfigurable computing card featuring the latest Xilinx Adaptive Compute Acceleration Platform (ACAP) platform with the Versal XCVC1902, a full FMC+ interface, PCIe Gen3x16 or 2xGen4x8 interface, two banks of DDR4-3200 each 72 bits wide (for 64 bits with 8 bits ECC), GEM0 Ethernet, QSPI, uSD, USB, UART, a Digilent PMOD site, one Samtec FireFly site capable of 28G/channel in either optical or copper cabling, and a robust system monitor.

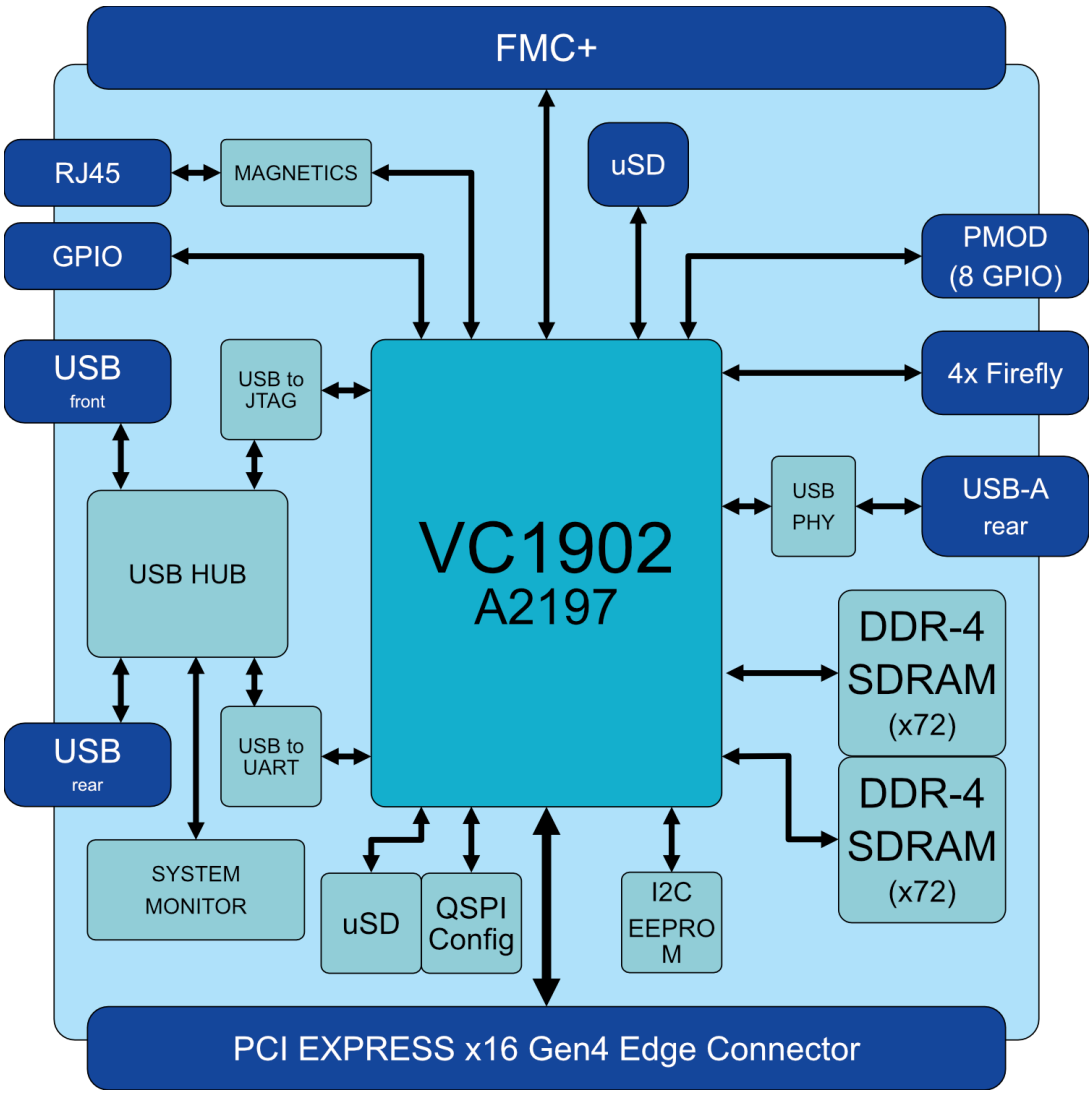

Figure 5 : ADM-PA100 Block Diagram

3.1.1 Switches

The ADM-PA100 has two octal DIP switch SW1 and SW2, located on the rear side of the board. The function of each switch is detailed below:

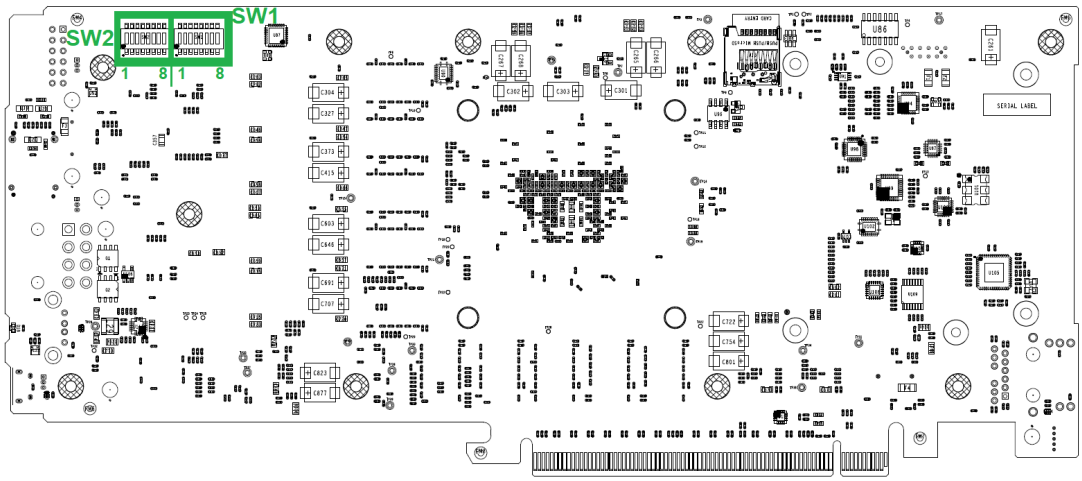

Figure 6 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	ON	BootMode 0	See Table 10	
SW1-2	OFF	BootMode 1	See Table 10	
SW1-3	OFF	BootMode 2	See Table 10	
SW1-4	OFF	BootMode 3	See Table 10	
SW1-5	OFF	Reserved	TBD	TBD
SW1-6	ON	12V Auto-detect	12V auto-detect enabled	8-pin ATX cable and PCIe edge both required
SW1-7	ON	Reserved	TBD	TBD
SW1-8	OFF	Power Off	Board will power up	Immediately power down
SW2-1	OFF	Factory Configuration	Normal operation	-
SW2-2	ON	Factory Configuration	-	Normal operation
SW2-3	OFF	HOST_I2C_EN	System Monitor connected to PCIe slot I2C	System Monitor isolated from PCIe slot I2C
SW2-4	OFF	Service Mode	System Monitor normal operation	System Monitor Service Mode (firmware update etc.)
SW2-5	OFF	PERST to POR_B	PCIE RESET isolated from POR_B	PCIE RESET will drive POR_B low
SW2-6	OFF	POR_B	ACAP power on reset released	ACAP power on reset active
SW2-7	OFF	User Switch 0	Pin G36 = '1'	Pin G36 = '0'
SW2-8	OFF	User Switch 1	Pin G37 = '1'	Pin G37 = '0'

Table 4 : Switch Functions

Use I/O Standard "LVCMOS15" when constraining the User Switch pins.

3.1.2 LEDs

There are 6 LEDs on the ADM-PA100, 2 of which are general purpose and whose meaning can be defined by the user. The other 4 have fixed functions described below:

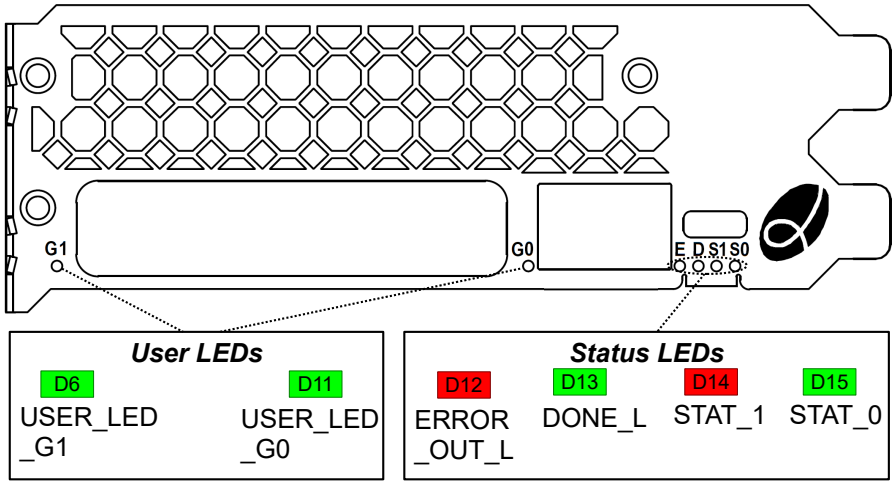

Figure 7 : Front Panel LEDs

Comp. Ref.	Function/Net Name	ON State	OFF State
D6	USER_LED_G1_1V8	User defined '0'	User defined '1'
D11	USER_LED_G0_1V8	User defined '0'	User defined '1'
D12	ERROR_OUT_L	Boot error	No error reported
D13	DONE_L	PL is configured	PL is not configured
D14	Status 1	See Status LED Definitions	
D15	Status 0	See Status LED Definitions	

Table 5 : LED Details

See Section Complete Pinout Table for full list of user controlled LED nets and pins

3.2 Clocking

The ADM-PA100 provides flexible reference clock solutions for the many multi-gigabit transceiver quads, DDR4 banks, and PL fabric. Any programmable clock (LMK61E2 or Si5338), is reconfigurable from the front panel Micro USB Interface by using Alpha Data's avr2util utility. This allows the user to configure almost any arbitrary clock frequency during application run time. The maximum clock frequency for rev3 and older PCBs (SN156 and lower) with the Si5338 is 350MHz. The maximum clock frequency for rev4 and newer PCBs (SN157 and higher) with the LMK61e2 is 900MHz. Customers who purchase RD-PA100 also have the option of embedding IP into their ACAP design that permits programmable clock reconfiguration via PCIe or from within the ACAP.

There is one available Si5328 jitter attenuator. This can provide clean and synchronous clocks to the FMC+ quad locations at many clock frequencies. These devices use volatile memory, so the ACAP design will need to reconfigure the register map over I2C after any power cycle.

All clock names in the section below can be found in Complete Pinout Table.

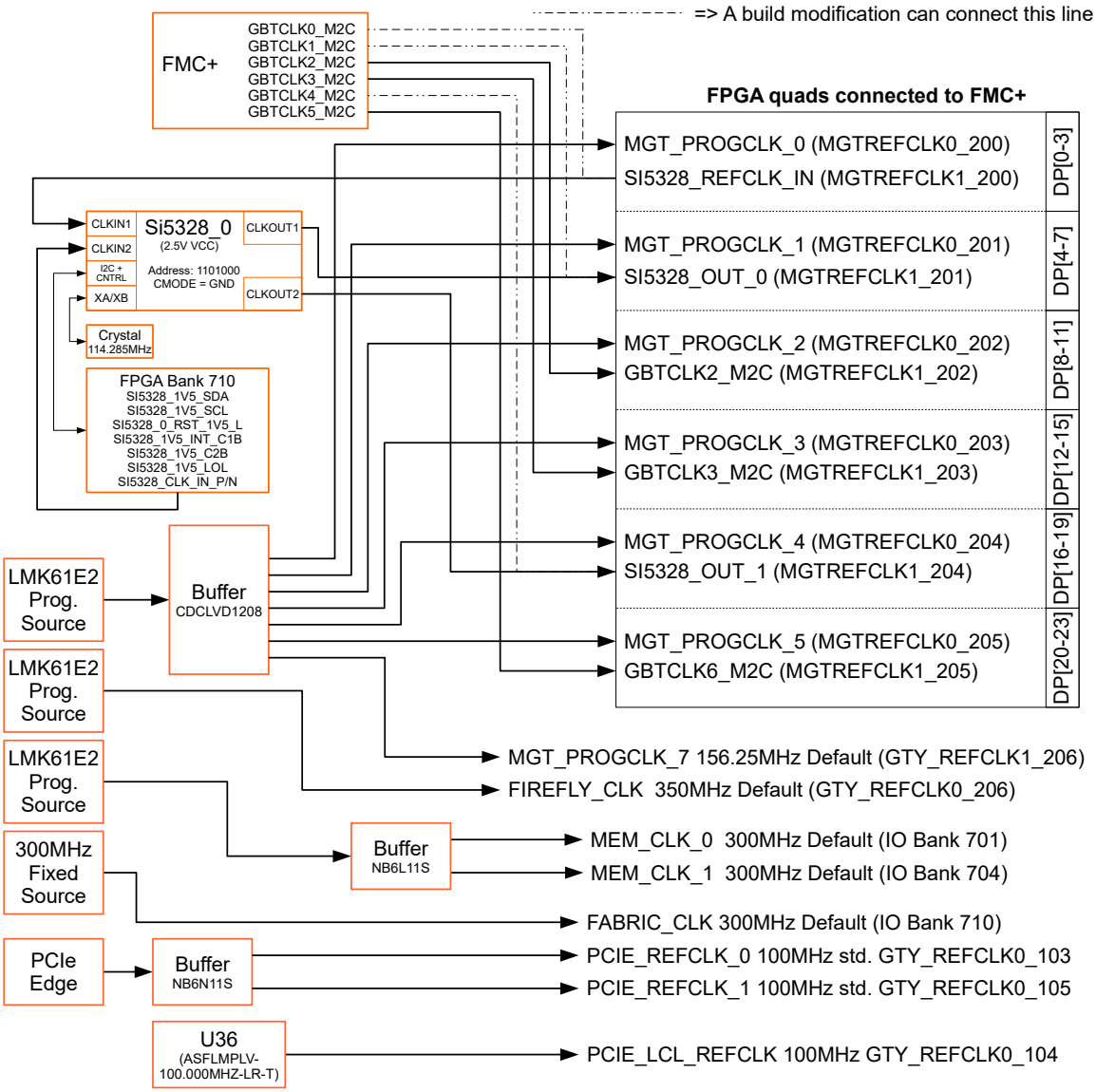

Figure 8 : Clock Topology Rev4+ (SN157 and newer)

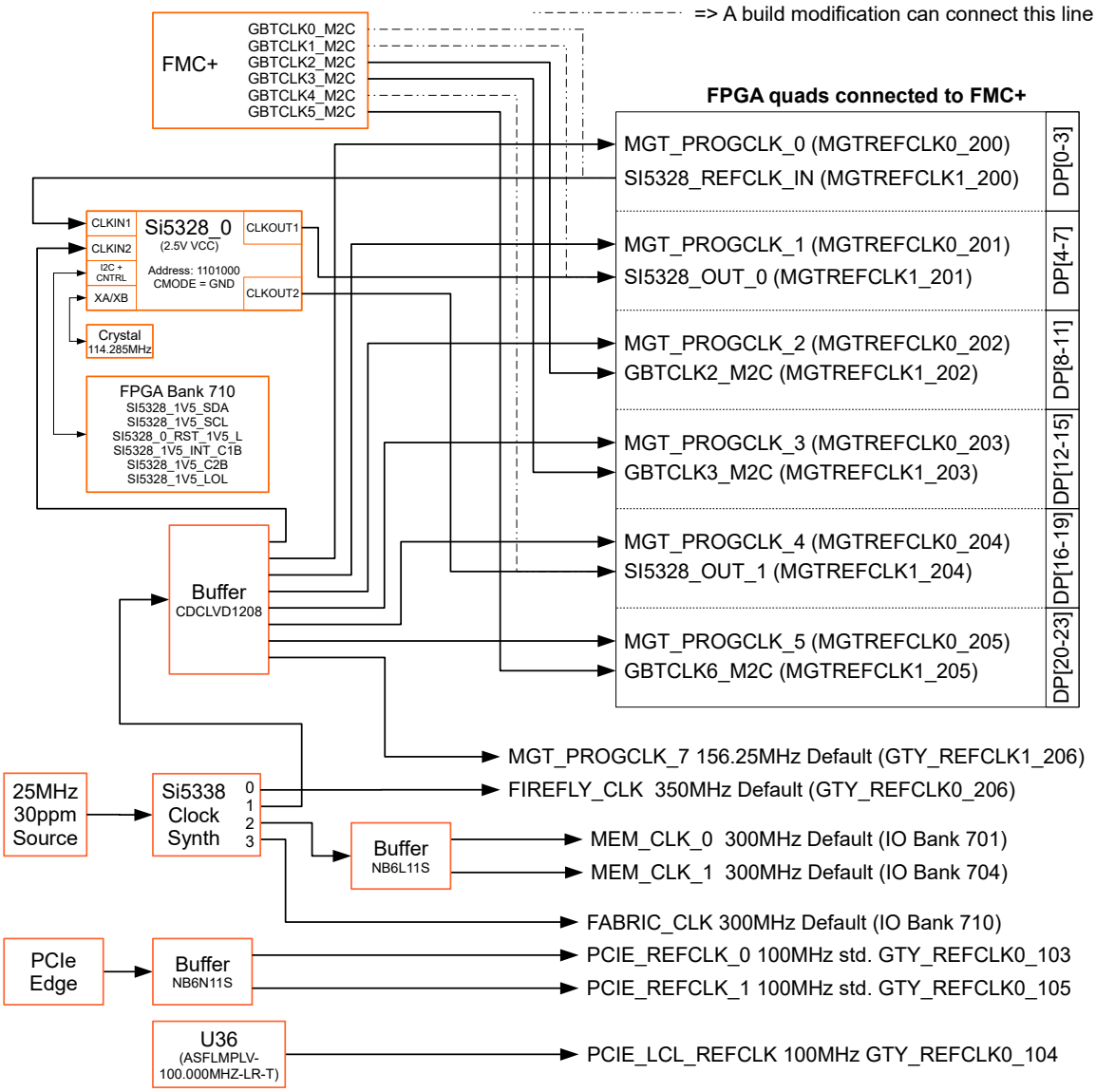

Figure 9 : Clock Topology Rev3- (SN156 and older)

3.2.1 LMK61E2

Rev4 and newer PCBs (SN157 and higher) use the LMK61E2 for arbitrary clock frequency synthesis. For complete technical details, please reference the datasheet:
https://www.ti.com/lit/ds/symlink/lmk61e2.pdf

The ADM-PA100 uses three LMK61E2 devices in the clock architecture. These can be accessed through either the USB or PCIe link using the AVR2UTIL application. See additional details on avr2util in the section: Micro USB Interface.

To re-program the LMK61E2 in a non-volatile manner, issue the following command:

```
avr2util <other options> setclknv-regmap <clock#> <reg. map file>
```

> **Note:**
> Each LMK61E2 is rated for only 100 non-volatile write operations.

To re-program the LMK61E2 in a volatile manner, issue the following command:

```
avr2util <other options> setclk-regmap <clock#> <reg. map file>
```

<other options> should be left blank for PCIE, and '-usbcom' for USB.

<clock#> is 0 for FIREFLY_CLK, 1 for MGT_PROGCLK, 2 for MEM_CLK.

<reg. map file> is a text file generated using the "LMK61xx Oscillator Programming Tool — SNAC074.ZIP" which can be obtained with a TI login from this page: https://www.ti.com/tool/LMK61E2EVM. After you have the tool installed, launch the application, type in the desired frequency, select "LVDS" output standard, click "Generate Configuration", then go to "File->Export hex register values"

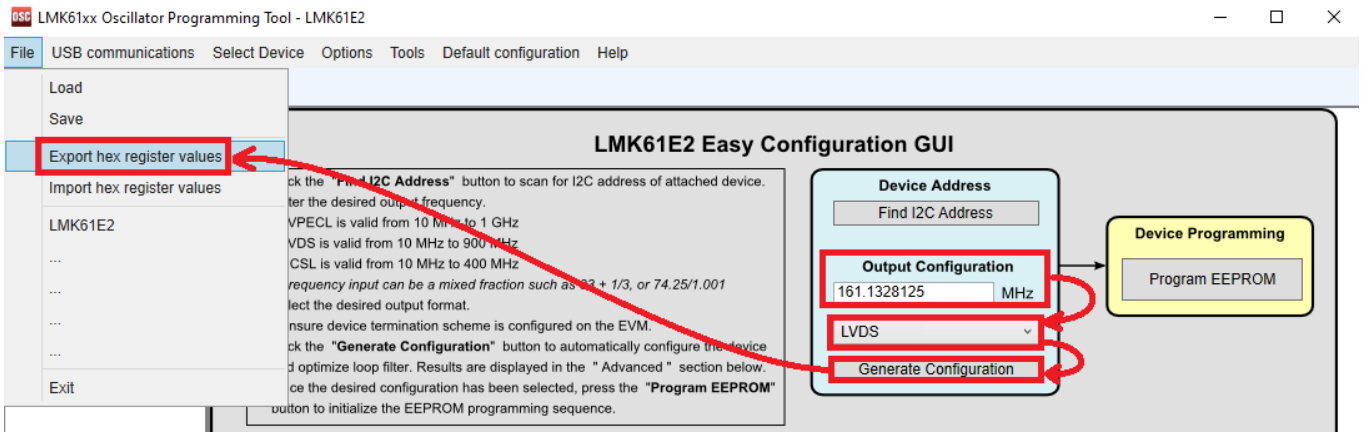

Figure 10 : LMK61xx Oscillator Programming Tool GUI

3.2.2 Si5338

Rev3 and older PCBs (SN156 and lower) use the Si5338 for arbitrary clock frequency synthesis. For complete technical details, please reference the datasheet:
https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/Si5338.pdf

This clock synthesizer can be accessed through either the USB or PCIe link using the AVR2UTIL application. See additional details on avr2util in the section: Micro USB Interface.

To re-program the Si5338 in a non-volatile manner, issue the following command:

```
avr2util <other options> setclknv <clock#> <freq>
```

To re-program the Si5338 in a volatile manner, issue the following command:

```
avr2util <other options> setclk <clock#> <freq>
```

<other options> should be left blank for PCIE, and '-usbcom' for USB.

<clock#> is 0 for FIREFLY_CLK, 1 for MGT_PROGCLK, 2 for MEM_CLK, 3 for FABRIC_CLK

<freq> is frequency in Hz

Here is an example of using USB to change the FIREFLY_CLK to 100MHz on the next power-up event:

```
avr2util.exe /usbcom com4 setclknv 0 100000000
```

3.2.3 Si5328

If jitter attenuation is required please see the reference documentation for the Si5328. www.silabs.com/Support%20Documents/TechnicalDocs/Si5328.pdf

There are two input clock options. For all revisions Si5328 pin CLKIN1 (board net name SI5328_REFCLK_IN_P/N) of the Si5328 is connected to an MGT clock output for the most direct clock recovery architecture. For rev4 and newer PCBs, Si5328 pin CLKIN2 (board net name SI5328_REFCLK_IN2_P/N) of the Si5328 is connected to an XPIO clock capable pin, allowing the application design to feed this clock from anywhere within the ACAP PL. For rev3 and older PCBs, Si5328 pin CLKIN2 (board net name MGT_PROGCLK_6_P/N) of the Si5328 is connected to a programable clock from the onboard clock synthesizer.

The two output clocks are connected to quads 201 and 204 to provide clocking capability to the entire FMC+ interface.

The INT_C1B and LOL signals for the Si5328 is available for use, and can be located at net names SI5328_1V5_INT_C1B and SI5328_1V5_LOL in the Complete Pinout Table.

The active low reset of the Si5328 is accessible to the ACAP. See net names SI5328_1V5_RST_L in the Complete Pinout Table.

> **Note:**
> Each sideband signal has an external pull-up resistor.

The Si5328 configuration register map is volatile, and must be written on each power up event over I2C. Use nets SI5328_1V5_SDA and SI5328_1V5_SCL at pins located in the Complete Pinout Table. The Si5328 device is configured the I2C address shown in the table below:

device	7bit Hex Address	Binary Address
Si5328	68	110_1000

Table 6 : Si5328 address table

3.2.4 PCIe Reference Clocks

The 16 MGT lanes connected to the PCIe card edge use MGT tiles 103 through 106 and use the host system's 100 MHz PCIe reference clock (net name PCIE_REFCLK_0_P/N or PCIE_REFCLK_1_P/N in the Complete Pinout Table).

Alternatively, a more stable but asynchronous onboard 100MHz clock is available as well (net name PCIE_LCL_REFCLK_P/N in the Complete Pinout Table).

3.2.5 Fabric Clock

The design offers a fabric clock (net name FABRIC_CLK_P/N) which defaults to 300 MHz. This clock is intended to be used for IDELAY elements in PL designs. The fabric clock is connected to a Global Clock (GC) pin. This clock frequency can be changed to any arbitrary clock frequency up to 350MHz by re-programming the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: Micro USB Interface.

Use constraints DIFF_TERM_ADV = TERM_100 and IOSTANDARD LVDS15 for this reference clock.

See net names FABRIC_CLK_P/N in the Complete Pinout Table for pin locations.

3.2.6 PS Reference Clock (PS_REF_CLK)

A 50MHz clock is fed into the dedicated REF_CLK_503 pin to drive the processor system.

3.2.7 MGT Programable Clock

The MGT reference clock connects to each quad connected to the FMC connector, the Si5328, and the FireFly quad. This programable clock has a default 156.25MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 350MHz by re-programming the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: Micro USB Interface.

See net names MGT_PROGCLK_*_PIN_P/N in the Complete Pinout Table for pin locations.

3.2.8 FMC Clocks

The FMC specification defines 6 gigabit transceiver clocks (GBTCLK*), one for each four high speed serial lanes. By default only GBTCLK2, GBTCLK3, and GBTCLK6 are connected. The other three can be connected through a build option custimzation.

The specification also defines 4 general clocks (CLK*_M2C and CLK*_BDIR). Each of these clocks have external AC coupling, DC bias, and 100 ohm termination (suitable for LVDS).

See ANSI/VITA 46.0 and ANSI/VITA 57.4 for full details of the FMC specification.

See net names GBTCLK*_PIN_P/N, CLK*_M2C_PIN_P/N, and CLK*_BIDIR_PIN_P/N in the Complete Pinout Table for pin locations.

The ACAP quads connected to the FMC site are also configured such that they can be clocked from the Si5328 jitter attenuator, or the onboard Si5338 clock synthesizer.

Pin locations of net names SI5328_*_OUT_P/N and MGT_PROGCLK_*_P/N can be located in the Complete Pinout Table.

3.2.9 Samtec FireFly Clock

The FireFly clock has a default 350MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 350MHz by re-programming the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: Micro USB Interface.

See net names FIREFLY_CLK_PIN_P/N in the Complete Pinout Table for pin locations.

3.2.10 Memory Clocks

Each of the two memory banks has their own buffered 300MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 350MHz by re-programming the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: Micro USB Interface.

See net names MEM_CLK_*_PIN_P/N in the Complete Pinout Table for pin locations.

See DDR4 SDRAM for mor information on the memory banks and their physical locations.

These clocks are not fabric accessible, but are reserved for the Versal DDR4 cores.

3.3 PCI Express

The ADM-PA100 is capable of PCIe Gen 1/2/3 with 1/4/8/16 lanes and Gen 4 with 1/4/8 lanes. The ACAP drives these lanes directly using the Integrated PCI Express block from Xilinx. Negotiation of PCIe link speed and number of lanes is generally automatic and does not require user intervention.

PCI Express reset (PERST#) is connected to the ACAP through a buffer. See Complete Pinout Table signal PERST_PL_L for fabric accessible location, and PCIE_RST_1V8_L for the PS location.

The pin assignments for the high speed lanes are provided in the pinout attached to the Complete Pinout Table, see net names PCIE_TX*_PIN_P/N and PCIE_RX*_P/N.

Note:
The ADM-PA100 has two PCIe lane configurations depending on the revision of the PCB. Rev4 and newer PCBs (SN157 and higher) are aligned with PCIe lane 0 in quad 103. Rev3 and older PCBs (SN156 and lower) are aligned with PCIe lane 0 in quad 106.

3.4 DDR4 SDRAM

Two banks of DDR4 SDRAM memory are soldered down to the board. The available density of the memory is 8GB/per bank, 16GB total. The memory interface is 72-bit wide data (64 data + 8 ECC). Maximum signalling rate is 3200 MT/s.

Memory solutions are available from the Xilinx (See Xilinx PG313 Versal ACAP Programmable Network on Chip and Integrated Memory Controller v1.0). DDR4_0 uses the Non-Flipped Pinout, and DDR4_1 uses the Flipped Pinout. An example memory exerciser project is included in the RD-PA100. All pin location information is included in Complete Pinout Table.

The components used are Micron MT40A1G16RC-062E or equivalent.

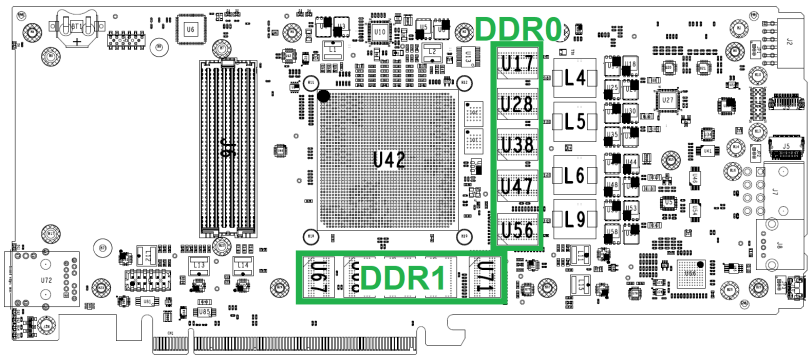

Figure 11 : DDR4 bank locations by index

Rev4 and later boards must use medium slew strengths to ensure error free memory operations. All revisions should use medium slew. Add constraints like the ones listed below to a project xdc file to implement this:

```
set_property SLEW MEDIUM [get_ports {c?_ddr4_dq*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_dm*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_act_n*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_adr*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_ba*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_bg*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_ck_*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_cke*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_cs_n*}]
set_property SLEW MEDIUM [get_ports {c?_ddr4_odt*}]
```

3.5 FMC+ Interface

The FMC+ interface provides a high-performance and flexible front-panel interface through a range of interchangeable industry standard IO modules.

The FMC+ interface adheres to VITA 57.4. The ADM-PA100 utilizes all possible FMC+ connectivity. This includes all GPIO, all MGT links, and all clock capable IO.

FMC I2C signal (SCL and SDA at C30 and C31) are connected to the system monitor microcontroller. They are used to determine operating voltage during start-up and are not accessible to the user directly, but can be accessed through the system monitor AVR2UTIL application.

Alpha Data provides a wide range of compatible FMC cards: Please see www.alpha-data.com/products/io-adaptors/, or contact **sales@alpha-data.com** for more details.

It is possible for Alpha Data to pre-fit the ADM-PA100 with FMC+ modules. Please contact **sales@alpha-data.com** for full details and options.

The FMC Present signal (PRSNT_M2C_L at connector pin H2) is connected to the system monitor microcontroller.

> **Note:**
> The ADM-PA100 supports only 1.5V and lower VADJ Voltages.

The ADM-PA100 provides additional keep out space in the FMC area to enable oversized FMC cards. This is ideal for pluggable optical modules like QSFP-DD. See Alpha Data FMC-PLUS-QSFP-DD for one example.

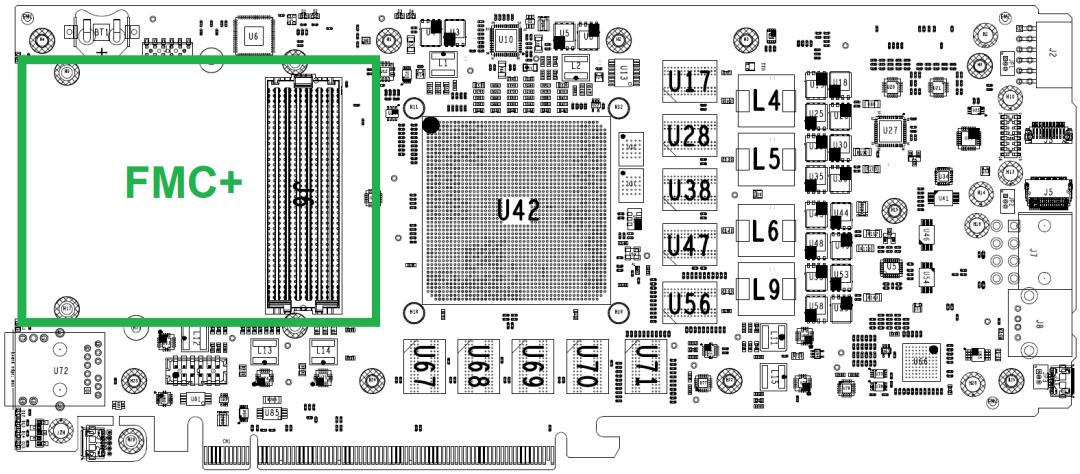

Figure 12 : FMC+ Location

The FMC+ site can be accessed by removing the top shroud. There are 13 M2 screws that need to be removed before the shroud will lift free. The default PA100 FMC bezel can also be removed by uninstalling the two M2.5 bezel screws on the bottom side of the PCB.

Note:
The ADM-PA100 is an ESD sensitive device. See Handling Instructions before handling the hardware.

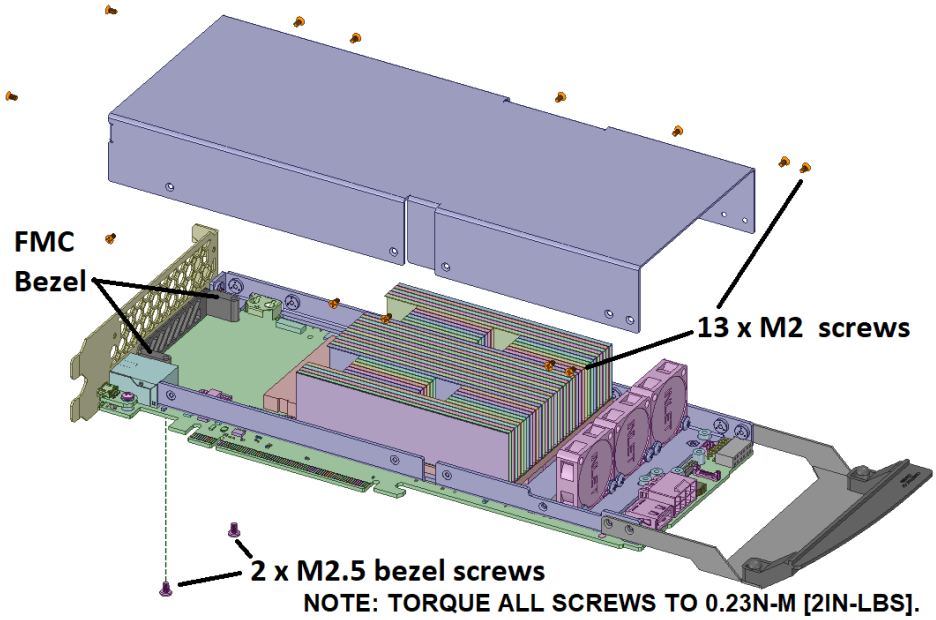

Figure 13 : FMC site access

The FMC+ Connector has GPIO connections arranged as follows:

Group	ACAP Bank	Net Name	Function
LA*	706 - 707	LA??_P/N	30x diff. pairs / 60x single-ended
		LA??_CC_P/N	4x global clocks / diff. pairs / 8 single-ended
HA*	708	HA??_P/N	21x diff. pairs / 42x single-ended
		HA??_CC_P/N	3x global clocks / diff. pairs / 6 single-ended
HB*	709	HB??_P/N	19x diff. pairs / 38x single-ended
		HB??_CC_P/N	3x diff. pairs / 6x single-ended
DP*	200 - 205	DP??_?2?_P/N	24x bidirection transceiver lanes

Table 7 : FMC+ Groups

FMC high speed pairs (net names DP*) are connected in sequential assending order with DP00* at quad 200 transceiver 0, and DP23* at quad 205 transceiver 3. See Complete Pinout Table for complete details and pin information.

3.6 FireFly

There is one FireFly site available on the circuit board. The site is capable of hosting either active optical or passive copper FireFly connectors. The communication interface can run at up to 28Gbps per channel in either cable type. There are 4 channels on the FireFly site (total maximum bandwidth of 114Gbps). This site is ideally suited for 4x 10G/25G, 1x 100G Ethernet, or any other protocol supported by the Xilinx GTY Transceivers. Please see Xilinx User Guide UG578 for more details on the capabilities of the transceivers.

All FireFly sites have control signals connected to the ACAP. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is FIREFLY* with locations clarified in the diagram below.

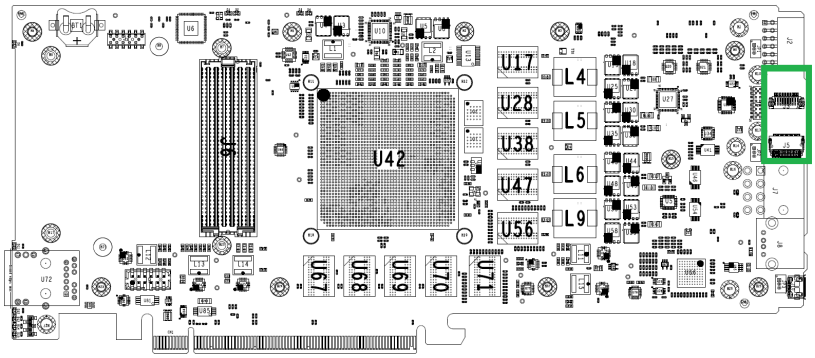

Figure 14 : FireFly Locations

The management interface of each FireFly module is connected directly to the ACAP. Each low speed sideband signals (MODPRS, INT_L, RST_L, SDA, SCL) has an external pull-up resistor.

3.7 System Monitor

The ADM-PA100 has the ability to monitor select temperatures, voltages, and currents in order to provide an indication of board health. The monitoring is implemented using an AVR microcontroller. This information can be read out via USB using the avr2util utility. Alternatively, the sensor information can be read directly by the ACAP or via PCIe if RD-PA100 is purchased (reference design package).

If the core ACAP temperature exceeds 105 degrees Celsius, the ACAP image will be cleared to prevent damage to the card.

Monitors	Identifier	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12V_AUX	ADC00	12V board input supply from 8-pin ATX Cable
12V_EDGE	ADC01	12V board input supply from PCIe Edge
12V_EDGE_I	ADC02	12V board input current from PCIe Edge in amps
3V3_AUX	ADC03	3.3V auxiliary board input supply from PCIE edge
3V3_DIG	ADC04	3.3V generated onboard for FMC and other circuits
3V3_VCCO	ADC05	3.3V generated onboard for ACAP IO voltage (VCCO)
1V8_DIG	ADC06	1.8V generated onboard for ACAP IO voltage (VCCO)
1V5_DIG	ADC07	1.5V generated onboard for ACAP IO voltage (VCCO)
1V5_AVCCAUX	ADC08	1.5V generated onboard for ACAP Aux voltage
1V2_AVTT	ADC09	1.2V generated onboard for transceiver Power (AVTT)
1V2_DIG	ADC10	1.2V generated onboard for SDRAM and ACAP (VCCO)
0V88_AVCC	ADC11	0.88V generated onboard for transceiver Power (AVCC)
VCC_INT	ADC12	0.8V generated onboard for ACAP core and AI power
FMC_VADJ	ADC13	1.0-1.5V generated onboard for FMC VADJ and ACAP (VCCO)
uC_Temp	TMP00	uC on-die temperature
Board0_Temp	TMP01	Board temperature near FMC connector (U24)
Board1_Temp	TMP02	Board temperature near back edge (U57)
ACAP_Temp	TMP03	ACAP on-die temperature

Table 8 : Voltage, Current, and Temperature Monitors

3.7.1 System Monitor Status LEDs

LEDs D14 (Red) and D15 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	ACAP configuration cleared to protect board

Table 9 : Status LED Definitions

3.8 Micro USB Interface

The ACAP can be configured directly from the USB connection on either the front panel or the rear card edge. The ADM-PA101 utilizes the Digilent USB-JTAG converter which is supported by the Xilinx software tool suite. Simply connect a micro-USB AB type cable between the ADM-PA101 USB port and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the ACAP and allow you to configure the ACAP and the SPI configuration Flash memory.

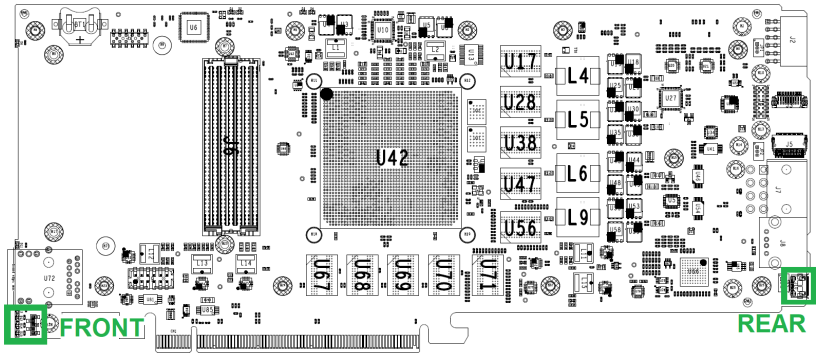

Figure 15 : USB Location

The same USB connector is used to directly access the system monitor system. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util for Windows and the associated USB driver is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use this command to see all options:

```
avr2util.exe /?
```

Use this command to display all sensor values:

```
avr2util.exe /usbcom com4 display-sensors
```

Here is an example of changing the FIREFLY_CLK to 100MHz on the next power-up event:

```
avr2util.exe /usbcom com4 setclknv 0 100000000
```

Setclk index 0 = FIREFLY_CLK, index 1 = MGT_PROGCLK, index 2 = MEM_CLK, index 3 = FABRIC_CLK.

Here is an example of changing the boot mode from uSD to QSPI on the next power-up event:

```
avr2util.exe /usbcom com4 set-boot-mode qspi24
```

Boot-mode commands use open drain drivers and can only drive mode pins low.

In the examples above, change 'com4' to match the com port number assigned under windows device manager.

3.9 Configuration

There are three main ways of configuring the ACAP on the ADM-PA100:

- From QSPI Flash memory, at power-on, as described in Section 3.9.1
- From uSD Flash memory, at power-on, as described in Section 3.9.2
- Using USB cable connected at either USB port Section 3.9.3

3.9.1 Configuration From QSPI Flash Memory

The ACAP can be automatically configured at power-on from two 1 Gbit QSPI flash memory devices configured as an x8 dual parallel SPI device (2x Micron part number MT25QU01GCBB8E12).

The ADM-PA100 is shipped with a simple PCIe endpoint bitstream which should be visible to the operating system (using Windows Device Manager or “lspci” in Linux) in order to provide confidence that the card is working correctly when installed in a system. On request, Alpha Data can pre-load custom bitstreams during production test. Please contact **sales@alpha-data.com** in order to discuss this possibility.

At power-on, the ACAP attempts to configure itself automatically according to the mode pins as described in Section 3.9.4. If the mode is set to QSPI24 or QSPI32, the ACAP will search on the header of the binary that has been flashed into the card. This normally results in SPIx8 configuration.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprogramming the ACAP. This provides a useful failsafe mechanism to re-program the ACAP even if it drops off the PCIe bus. The system monitor can be accessed with avr2util over USB at the front panel and rear edge.

3.9.1.1 Building and Programming QSPI Configuration Images

You can start with one of the example Vivado projects(.xpr format) that are available for customers in the early access section of the PA100. You can request access to them by messaging **support@alpha-data.com**

Every early access project contain the implementation results of the example design in question, so you can use Hardware Manager to program the FPGA binary directly. Below are described the steps to do a QSPI Flash programming. You would need to set up the equipment first:

- Connect the PA100 to a PCIe slot of a host PC
- Make sure SW1-1, SW1-2, SW1-3, SW1-4 are all ON in the PA100 (see Switches)
- Connect an USB cable between a test PC and the PA100's micro-USB connector
- Turn on the host PC with the PA100 connected to it

Now, it is time run the actual flash programming commands through Vivado's GUI:

- Open Vivado -> Open Project(select .xpr file) -> Select HW Manager -> Open Target -> Auto Connect
- Right click on xcvc1902_1 -> Add Configuration Memory Device -> search for 'cfgmem-qspi-x8-dual_parallel', selecting it -> click OK
- A message asking the user to configure the device now will pop up. Click OK accepting it
- Now, copy the path to the PDI image in the 'Initialization PDI' field, and click OK. This will program the QSPI Flash with the example design that you have opened. If you have a .BIN file instead, use the path for that binary file and leave the other fields as are

If you followed the previous steps, the FPGA should have been correctly configured. In order to test that, turn the host PC with the PA100 OFF, change the switches SW1-1, SW1-3, SW1-4 ON and SW1-2 OFF. Then turn the host PC back ON. You should see both DONE_L and STAT_0 LEDs ON after a few seconds(see LEDs)

3.9.2 Configuration From uSD Flash Memory

The ACAP can be automatically configured at power-on from the Micro Secure Digital card (uSD) slot along the north edge of the card.

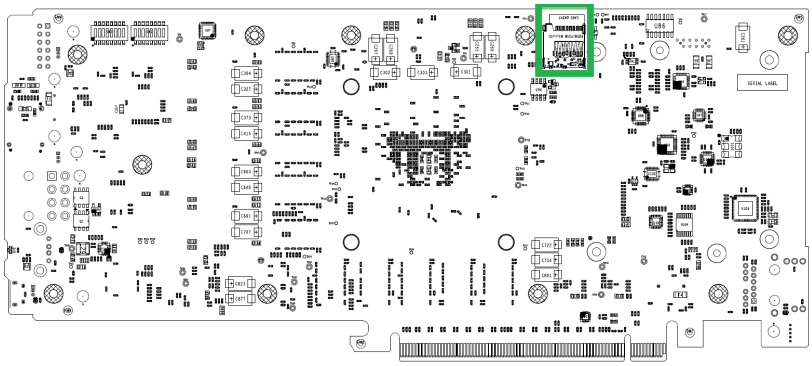

Figure 16 : uSD Location

The ADM-PA100 is shipped with a simple PCIe endpoint bitstream which should be visible to the operating system (using Windows Device Manager or “lspci” in Linux) in order to provide confidence that the card is working correctly when installed in a system. On request, Alpha Data can pre-load custom bitstreams during production test. Please contact **sales@alpha-data.com** in order to discuss this possibility.

At power-on, the ACAP attempts to configure itself automatically according to the mode pins as described in Section 3.9.4. Alpha Data ships these cards set to the uSD boot mode by default.

3.9.2.1 Building and Programming uSD Configuration Images

Find below the steps to get a bootable image file(BOOT.BIN) from your implemented example design,

- Prepare the uSD card by formatting it as a whole FAT partition.
- Find the generated PDI file of your design(implementation folder of the project).
- Copy the .pdi to FAT32 SD card and rename it to BOOT.bin

The uSD card is now ready to be booted from, so you can insert it in the PA100 with the right boot mode in the switches and turn it on. Your example design will be programmed in the FPGA automatically at boot.

3.9.3 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel or rear edge USB port. This permits the ACAP to be reconfigured using the Xilinx Vivado Hardware Manager and Vitis via the integrated Digilent JTAG converter box. The device will be automatically recognized in Vivado Hardware Manager and Vitis.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of Xilinx UG908

Also, if you went through the section Building and Programming QSPI Configuration Images, you can program the FPGA(xcvc1902 part) instead of the Flash attached to it. The HW setup is the same. You simply don't need to turn OFF and ON the Host PC after programming the FPGA.

3.9.4 Boot Modes

MODE3 (SW1-4)	MODE2 (SW1-3)	MODE1 (SW1-2)	MODE0 (SW1-1)	Boot Mode
ON	ON	ON	ON	JTAG
ON	ON	ON	OFF	Quad SPI (24 bit addressing)
ON	ON	OFF	ON	Quad SPI (32 bit addressing)
OFF	OFF	OFF	ON	SD Flash - SD 3.0

Table 10 : Boot Mode Selection

Note: all other possible switch settings are reserved / invalid.

The system monitor also has the ability to control the mode pins, enabling remote changes to boot device for golden image fallback and recovery. The system monitor can drive the MODE pins low (open drain drive), so it is recommended to leave the switches in the OFF positions or set to SD 3.0 boot mode. From there, the user can issue commands to change the boot mode between "sd1_v3" or "qspi32" and then reboot the board:

Loading an image from qspi32 remotely:

- avr2util.exe -usbcom com4 set-boot-mode qspi32
- avr2util.exe -usbcom com4 set-brd-power off
- avr2util.exe -usbcom com4 set-brd-power on

Use set-boot-mode to immediately change boot mode settings. Use set-boot-mode-nv to change boot mode setting in a non-volatile manner after a complete system power cycle.

3.10 ULPI USB Interface

The MIO ULPI USB interface is instantiated. See MIO Map

Part number USB3320C-EZK is used for PHY electrical conversion. This PHY is capable of USB 2.0 communication speeds. An onboard supply provides 5V @ 500mA on the VBUS pin of the USB receptacle. The location of the USB PHY is located along the back edge of the card.

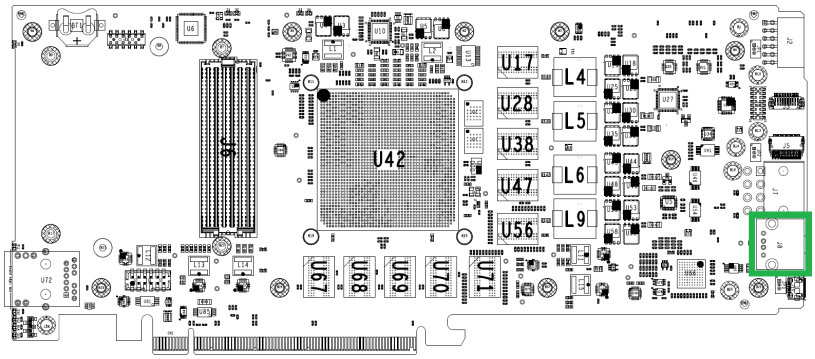

Figure 17 : ULPI USB Location

3.11 UART interfaces

UART0 and UART1 interfaces are available. See MIO Map

Both of these UART interfaces are brought out through the onboard USB hub which can be accessed at either the front or the back edge of the card.

UART0 passes through an FT2232HQ USB to UART converter. This is the same IC that performs the USB to JTAG conversion. This UART interface will not appear in the system until after the board is fully powered and is not suitable to capture power-on messages from the processor.

UART1 passes through an FT230XQ USB to UART converter. This device is powered from the USB VBUS supply provided by the USB cable. This UART interface will appear in the host system as soon as the USB cable is installed, even before the ADM-PA100 is powered up. This interface is suitable to capture power-on messages from the processor.

3.12 GEM0

The Gigabit Ethernet Manager (GEM0) is interfaced with a Microchip VSC8541 in rev4+ (SN157 and higher) PCBs and Marvell 88E1512 in rev3- (SN156 and lower) to provide 10/100/1000 Base-T Ethernet to the ACAP. This interface is accessible at the front panel.

A dedicated reset signal is connected to the MIO pins, see signal name GEM0_RST_L in Complete Pinout Table. This pin has an external pull-up and its use is optional.

See MIO Map

For rev4+: The Ethernet jack has two LED colors available. They are mapped to the VSC8541 PHY LED[*] pins and their function is user defined over the GEM0_MDIO interface. The LED mapping is: green->LED[0], orange-> LED[1]

For rev3-: The Ethernet jack has three LED colors available. They are mapped to the 88E1512 PHY LED[*] pins and their function is user defined over the GEM0_MDIO interface. The LED mapping is: green->LED[0], orange-> LED[1], yellow->LED[3].

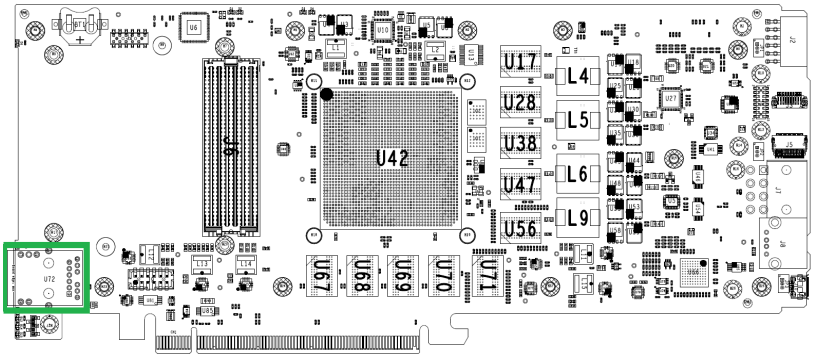

Figure 18 : GEM0 Ethernet Location

3.13 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number CAT34C02HU4IGT4A

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP, SPARE_SCL, and SPARE_SDA respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

3.14 PMOD

The ADM-PA100 includes a twelve-pin right angle connector PMOD host interface at the rear edge of the card with a full 0.9" clearance. This interface is connected to the PL of the ACAP.

See the PMOD Specification for full details.

Signals from this interface start with the name PMOD* and can be found in Complete Pinout Table.

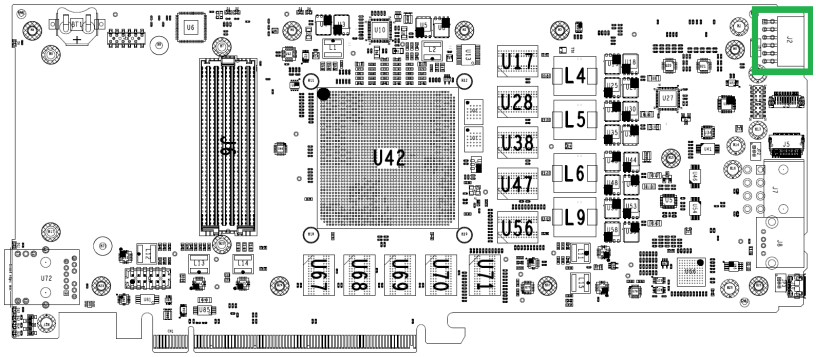

Figure 19 : PMOD location

3.15 Battery

The ADM-PA100 includes a battery cage that powers VCC_BATT (ACAP pin AG33). This cage is Keystone 3096 holder. Use with SR44 batteries with a nominal voltage of 1.55V.

The battery includes a 470uF capacitor in parallel to hold charge during a brief battery change operation.

Install the battery through the opening along the side of the stiffening plates.

A battery is not included.

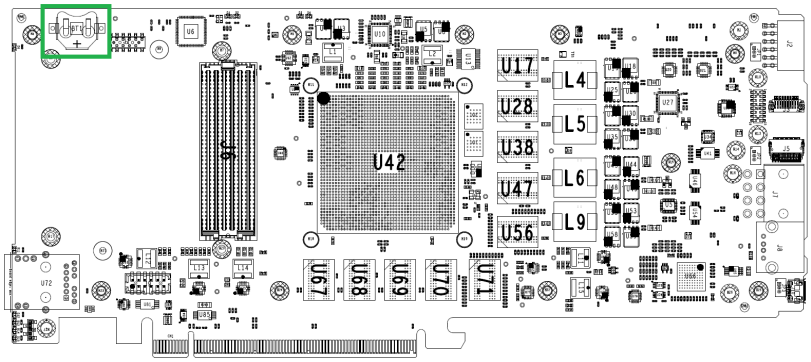

Figure 20 : Battery Location

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Appendix A: MIO Map

Pin Number	Pin Name	Signal Name	Comment
F34	PMC_MIO0_500	QSPI0_CLK	Dual-Parallel Quad SPI
G34	PMC_MIO1_500	QSPI0_IO[1]	Dual-Parallel Quad SPI
H33	PMC_MIO2_500	QSPI0_IO[2]	Dual-Parallel Quad SPI
F33	PMC_MIO3_500	QSPI0_IO[3]	Dual-Parallel Quad SPI
E33	PMC_MIO4_500	QSPI0_IO[0]	Dual-Parallel Quad SPI
F32	PMC_MIO5_500	QSPI0_CS_b	Dual-Parallel Quad SPI
G32	PMC_MIO6_500	NC	ERROR
H32	PMC_MIO7_500	QSPI1_CS_b	Dual-Parallel Quad SPI
K32	PMC_MIO8_500	QSPI1_IO[0]	Dual-Parallel Quad SPI
L32	PMC_MIO9_500	QSPI1_IO[1]	Dual-Parallel Quad SPI
M32	PMC_MIO10_500	QSPI1_IO[2]	Dual-Parallel Quad SPI
N32	PMC_MIO11_500	QSPI1_IO[3]	Dual-Parallel Quad SPI
N31	PMC_MIO12_500	QSPI1_CLK	Dual-Parallel Quad SPI
M31	PMC_MIO13_500	USB_ULPI_RST	USB 2.0
K31	PMC_MIO14_500	USB_ULPI_DATA[0]	USB 2.0
J31	PMC_MIO15_500	USB_ULPI_DATA[1]	USB 2.0
H31	PMC_MIO16_500	USB_ULPI_DATA[2]	USB 2.0
G31	PMC_MIO17_500	USB_ULPI_DATA[3]	USB 2.0
F30	PMC_MIO18_500	USB_ULPI_CLK	USB 2.0
G30	PMC_MIO19_500	USB_ULPI_DATA[4]	USB 2.0
J30	PMC_MIO20_500	USB_ULPI_DATA[5]	USB 2.0
K30	PMC_MIO21_500	USB_ULPI_DATA[6]	USB 2.0
L30	PMC_MIO22_500	USB_ULPI_DATA[7]	USB 2.0
M30	PMC_MIO23_500	USB_ULPI_DIR	USB 2.0
M29	PMC_MIO24_500	USB_ULPI_STP	USB 2.0
L29	PMC_MIO25_500	USB_ULPI_NXT	USB 2.0
B21	PMC_MIO26_501	SD1_CLK	SD1_3.0
C21	PMC_MIO27_501	SD1_DIR1	SD1_3.0
D21	PMC_MIO28_501	SD1_DETECT	SD1_3.0
E21	PMC_MIO29_501	SD1_CMD	SD1_3.0
F20	PMC_MIO30_501	SD1_DATA[0]	SD1_3.0
E20	PMC_MIO31_501	SD1_DATA[1]	SD1_3.0
D20	PMC_MIO32_501	SD1_DATA[2]	SD1_3.0
B20	PMC_MIO33_501	SD1_DATA[3]	SD1_3.0

Table 11 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
A20	PMC_MIO34_501	SD1_SEL	SD1_3.0
A19	PMC_MIO35_501	SD1_DIR_CMD	SD1_3.0
B19	PMC_MIO36_501	SD1_ DIR0	SD1_3.0
C19	PMC_MIO37_501	GEM0_RST_L	GEM0 Ethernet
D19	PMC_MIO38_501	PCIE_PERST_B	PCIE
F19	PMC_MIO39_501	NC (Rev3 and older) PCIE_PERST_B (Rev4 and newer)	PCIE
G19	PMC_MIO40_501	NC	ERROR
F18	PMC_MIO41_501	NC	ERROR
E18	PMC_MIO42_501	UART0_RXD	Not availabe until full power
D18	PMC_MIO43_501	UART0_TXD	Not availabe until full power
C18	PMC_MIO44_501	SYSMON_I2C_SCL	Not Used
A18	PMC_MIO45_501	SYSMON_I2C_SDA	Not Used
A17	PMC_MIO46_501	UART1_RXD	Available with aux. power
B17	PMC_MIO47_501	UART1_TXD	Available with aux. power
C17	PMC_MIO48_501	LPD_I2C1_SCL	Not Used
E17	PMC_MIO49_501	LPD_I2C1_SDA	Not Used
F17	PMC_MIO50_501	PMC_I2C_SCL	Not Used
G17	PMC_MIO51_501	PMC_I2C_SDA	Not Used
A39	LPD_MIO0_502	GEM0_TX_CLK	GEM0 Ethernet
B39	LPD_MIO1_502	GEM0_TX_DATA[0]	GEM0 Ethernet
C39	LPD_MIO2_502	GEM0_TX_DATA[1]	GEM0 Ethernet
C38	LPD_MIO3_502	GEM0_TX_DATA[2]	GEM0 Ethernet
A38	LPD_MIO4_502	GEM0_TX_DATA[3]	GEM0 Ethernet
A37	LPD_MIO5_502	GEM0_TX_CTRL	GEM0 Ethernet
B37	LPD_MIO6_502	GEM0_RX_CLK	GEM0 Ethernet
C37	LPD_MIO7_502	GEM0_RX_DATA[0]	GEM0 Ethernet
E37	LPD_MIO8_502	GEM0_RX_DATA[1]	GEM0 Ethernet
F37	LPD_MIO9_502	GEM0_RX_DATA[2]	GEM0 Ethernet
E36	LPD_MIO10_502	GEM0_RX_DATA[3]	GEM0 Ethernet
D36	LPD_MIO11_502	GEM0_RX_CTRL	GEM0 Ethernet
C36	LPD_MIO12_502	GPIO	GPIO J4 at rear
B36	LPD_MIO13_502	GPIO	GPIO J4 at rear
A35	LPD_MIO14_502	GPIO	GPIO J4 at rear
B35	LPD_MIO15_502	GPIO	GPIO J4 at rear
D35	LPD_MIO16_502	GPIO	GPIO J4 at rear

Table 11 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
E35	LPD_MIO17_502	GPIO	GPIO J4 at rear
F35	LPD_MIO18_502	GPIO	GPIO J4 at rear
G35	LPD_MIO19_502	GPIO	GPIO J4 at rear
D34	LPD_MIO20_502	GPIO	GPIO J4 at rear
C34	LPD_MIO21_502	GPIO	GPIO J4 at rear
B34	LPD_MIO22_502	GPIO	GPIO J4 at rear
A34	LPD_MIO23_502	GPIO	GPIO J4 at rear
C33	LPD_MIO24_502	GEM0_MDIO_CLK	GEM0 Ethernet
D33	LPD_MIO25_502	GEM0_MDIO_DATA	GEM0 Ethernet

Table 11 : MIO Map

Appendix B: Complete Pinout Table

Pin Number	Signal Name	Pin Name	IO Voltage
M17	AVR_B2U	IO_L1P_406	1.5
M19	AVR_MON_CLK	IO_L2P_406	1.5
L17	AVR_U2B	IO_L1N_406	1.5
BB24	CLK0_M2C_PIN_N	IO_L24N_GC_XCC_N8P1_M2P49_706	1.5
BA24	CLK0_M2C_PIN_P	IO_L24P_GC_XCC_N8P0_M2P48_706	1.5
BA12	CLK1_M2C_PIN_N	IO_L24N_GC_XCC_N8P1_M2P157_708	1.5
AY13	CLK1_M2C_PIN_P	IO_L24P_GC_XCC_N8P0_M2P156_708	1.5
BD22	CLK2_BIDIR_PIN_N	IO_L9N_GC_XCC_N3P1_M2P19_706	1.5
BC23	CLK2_BIDIR_PIN_P	IO_L9P_GC_XCC_N3P0_M2P18_706	1.5
AW23	CLK3_BIDIR_PIN_N	IO_L12N_GC_XCC_N4P1_M2P25_706	1.5
AV23	CLK3_BIDIR_PIN_P	IO_L12P_GC_XCC_N4P0_M2P24_706	1.5
AE38	DDR4_0_A0	IO_L18P_XCC_N6P0_M0P36_700	1.2
AD41	DDR4_0_A1	IO_L17N_N5P5_M0P35_700	1.2
AF38	DDR4_0_A10	IO_L21N_XCC_N7P1_M0P43_700	1.2
AD42	DDR4_0_A11	IO_L25P_N8P2_M0P50_700	1.2
AF46	DDR4_0_A12	IO_L0N_XCC_N0P1_M0P1_700	1.2
AF43	DDR4_0_A13	IO_L24N_GC_XCC_N8P1_M0P49_700	1.2
AJ40	DDR4_0_A14	IO_L16N_N5P3_M0P33_700	1.2
AH41	DDR4_0_A15	IO_L14N_N4P5_M0P29_700	1.2
AE40	DDR4_0_A2	IO_L17P_N5P4_M0P34_700	1.2
AG37	DDR4_0_A3	IO_L20P_N6P4_M0P40_700	1.2
AF39	DDR4_0_A4	IO_L12P_GC_XCC_N4P0_M0P24_700	1.2
AF42	DDR4_0_A5	IO_L26P_N8P4_M0P52_700	1.2
AE42	DDR4_0_A6	IO_L24P_GC_XCC_N8P0_M0P48_700	1.2
AG44	DDR4_0_A7	IO_L6N_GC_XCC_N2P1_M0P13_700	1.2
AD43	DDR4_0_A8	IO_L25N_N8P3_M0P51_700	1.2
AC37	DDR4_0_A9	IO_L19P_N6P2_M0P38_700	1.2
AF37	DDR4_0_ACT_N	IO_L18N_XCC_N6P1_M0P37_700	1.2
AL42	DDR4_0_ALERT_N	IO_L25N_N8P3_M0P105_701	1.2
AH38	DDR4_0_BA0	IO_L20N_N6P5_M0P41_700	1.2
AF40	DDR4_0_BA1	IO_L12N_GC_XCC_N4P1_M0P25_700	1.2
AG39	DDR4_0_BG0	IO_L21P_XCC_N7P0_M0P42_700	1.2
AD38	DDR4_0_CKE	IO_L23P_N7P4_M0P46_700	1.2

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
AF41	DDR4_0_CLK_C	IO_L15N_XCC_N5P1_M0P31_700	1.2
AG41	DDR4_0_CLK_T	IO_L15P_XCC_N5P0_M0P30_700	1.2
AH40	DDR4_0_CS_N	IO_L14P_N4P4_M0P28_700	1.2
AN42	DDR4_0_DEBUG	IO_L26P_N8P4_M0P106_701	1.2
AP40	DDR4_0_DM0	IO_L18P_XCC_N6P0_M0P90_701	1.2
AK40	DDR4_0_DM1	IO_L12P_GC_XCC_N4P0_M0P78_701	1.2
AF47	DDR4_0_DM2	IO_L0P_XCC_N0P0_M0P0_700	1.2
AH43	DDR4_0_DM3	IO_L6P_GC_XCC_N2P0_M0P12_700	1.2
AN46	DDR4_0_DM4	IO_L0P_XCC_N0P0_M0P54_701	1.2
AT47	DDR4_0_DM5	IO_L9P_GC_XCC_N3P0_M0P72_701	1.2
BB46	DDR4_0_DM6	IO_L3P_XCC_N1P0_M0P114_702	1.2
AY45	DDR4_0_DM7	IO_L6P_GC_XCC_N2P0_M0P120_702	1.2
AY42	DDR4_0_DM8	IO_L12P_GC_XCC_N4P0_M0P132_702	1.2
AT40	DDR4_0_DQ0	IO_L22P_N7P2_M0P98_701	1.2
AN40	DDR4_0_DQ1	IO_L23N_N7P5_M0P101_701	1.2
AM40	DDR4_0_DQ10	IO_L16N_N5P3_M0P87_701	1.2
AM38	DDR4_0_DQ11	IO_L17N_N5P5_M0P89_701	1.2
AM41	DDR4_0_DQ12	IO_L14N_N4P5_M0P83_701	1.2
AK37	DDR4_0_DQ13	IO_L13P_N4P2_M0P80_701	1.2
AM39	DDR4_0_DQ14	IO_L16P_N5P2_M0P86_701	1.2
AK38	DDR4_0_DQ15	IO_L13N_N4P3_M0P81_701	1.2
AK46	DDR4_0_DQ16	IO_L4P_N1P2_M0P8_700	1.2
AE46	DDR4_0_DQ17	IO_L1N_N0P3_M0P3_700	1.2
AH47	DDR4_0_DQ18	IO_L2P_N0P4_M0P4_700	1.2
AE47	DDR4_0_DQ19	IO_L5N_N1P5_M0P11_700	1.2
AR39	DDR4_0_DQ2	IO_L20P_N6P4_M0P94_701	1.2
AK47	DDR4_0_DQ20	IO_L4N_N1P3_M0P9_700	1.2
AD47	DDR4_0_DQ21	IO_L5P_N1P4_M0P10_700	1.2
AJ47	DDR4_0_DQ22	IO_L2N_N0P5_M0P5_700	1.2
AD45	DDR4_0_DQ23	IO_L1P_N0P2_M0P2_700	1.2
AJ44	DDR4_0_DQ24	IO_L8P_N2P4_M0P16_700	1.2
AE45	DDR4_0_DQ25	IO_L11N_N3P5_M0P23_700	1.2
AK45	DDR4_0_DQ26	IO_L10N_N3P3_M0P21_700	1.2
AF44	DDR4_0_DQ27	IO_L11P_N3P4_M0P22_700	1.2
AK44	DDR4_0_DQ28	IO_L10P_N3P2_M0P20_700	1.2
AD44	DDR4_0_DQ29	IO_L7P_N2P2_M0P14_700	1.2

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
AP39	DDR4_0_DQ3	IO_L23P_N7P4_M0P100_701	1.2
AJ45	DDR4_0_DQ30	IO_L8N_N2P5_M0P17_700	1.2
AE44	DDR4_0_DQ31	IO_L7N_N2P3_M0P15_700	1.2
AL44	DDR4_0_DQ32	IO_L4N_N1P3_M0P63_701	1.2
AM46	DDR4_0_DQ33	IO_L5P_N1P4_M0P64_701	1.2
AM45	DDR4_0_DQ34	IO_L2N_N0P5_M0P59_701	1.2
AL46	DDR4_0_DQ35	IO_L1P_N0P2_M0P56_701	1.2
AL43	DDR4_0_DQ36	IO_L4P_N1P2_M0P62_701	1.2
AL47	DDR4_0_DQ37	IO_L1N_N0P3_M0P57_701	1.2
AM44	DDR4_0_DQ38	IO_L2P_N0P4_M0P58_701	1.2
AN47	DDR4_0_DQ39	IO_L5N_N1P5_M0P65_701	1.2
AT39	DDR4_0_DQ4	IO_L20N_N6P5_M0P95_701	1.2
AU46	DDR4_0_DQ40	IO_L10N_N3P3_M0P75_701	1.2
AP44	DDR4_0_DQ41	IO_L7N_N2P3_M0P69_701	1.2
AU45	DDR4_0_DQ42	IO_L10P_N3P2_M0P74_701	1.2
AR45	DDR4_0_DQ43	IO_L11N_N3P5_M0P77_701	1.2
AU44	DDR4_0_DQ44	IO_L8N_N2P5_M0P71_701	1.2
AP43	DDR4_0_DQ45	IO_L7P_N2P2_M0P68_701	1.2
AT44	DDR4_0_DQ46	IO_L8P_N2P4_M0P70_701	1.2
AR44	DDR4_0_DQ47	IO_L11P_N3P4_M0P76_701	1.2
BD47	DDR4_0_DQ48	IO_L4N_N1P3_M0P117_702	1.2
AW47	DDR4_0_DQ49	IO_L5N_N1P5_M0P119_702	1.2
AN38	DDR4_0_DQ5	IO_L19N_N6P3_M0P93_701	1.2
BC46	DDR4_0_DQ50	IO_L2P_N0P4_M0P112_702	1.2
AY46	DDR4_0_DQ51	IO_L5P_N1P4_M0P118_702	1.2
BE46	DDR4_0_DQ52	IO_L4P_N1P2_M0P116_702	1.2
AV46	DDR4_0_DQ53	IO_L1P_N0P2_M0P110_702	1.2
BC47	DDR4_0_DQ54	IO_L2N_N0P5_M0P113_702	1.2
AV47	DDR4_0_DQ55	IO_L1N_N0P3_M0P111_702	1.2
BD44	DDR4_0_DQ56	IO_L10P_N3P2_M0P128_702	1.2
AW44	DDR4_0_DQ57	IO_L7P_N2P2_M0P122_702	1.2
BD45	DDR4_0_DQ58	IO_L8N_N2P5_M0P125_702	1.2
AY44	DDR4_0_DQ59	IO_L11P_N3P4_M0P130_702	1.2
AT41	DDR4_0_DQ6	IO_L22N_N7P3_M0P99_701	1.2
BE45	DDR4_0_DQ60	IO_L10N_N3P3_M0P129_702	1.2
AV45	DDR4_0_DQ61	IO_L7N_N2P3_M0P123_702	1.2

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
BC45	DDR4_0_DQ62	IO_L8P_N2P4_M0P124_702	1.2
AW45	DDR4_0_DQ63	IO_L11N_N3P5_M0P131_702	1.2
BD42	DDR4_0_DQ64	IO_L16P_N5P2_M0P140_702	1.2
AW42	DDR4_0_DQ65	IO_L17P_N5P4_M0P142_702	1.2
BC43	DDR4_0_DQ66	IO_L14N_N4P5_M0P137_702	1.2
AW43	DDR4_0_DQ67	IO_L17N_N5P5_M0P143_702	1.2
BE42	DDR4_0_DQ68	IO_L16N_N5P3_M0P141_702	1.2
AV43	DDR4_0_DQ69	IO_L13N_N4P3_M0P135_702	1.2
AM37	DDR4_0_DQ7	IO_L19P_N6P2_M0P92_701	1.2
BC42	DDR4_0_DQ70	IO_L14P_N4P4_M0P136_702	1.2
AV42	DDR4_0_DQ71	IO_L13P_N4P2_M0P134_702	1.2
AL41	DDR4_0_DQ8	IO_L14P_N4P4_M0P82_701	1.2
AL37	DDR4_0_DQ9	IO_L17P_N5P4_M0P88_701	1.2
AR41	DDR4_0_DQS0_C	IO_L21N_XCC_N7P1_M0P97_701	1.2
AR42	DDR4_0_DQS0_T	IO_L21P_XCC_N7P0_M0P96_701	1.2
AK39	DDR4_0_DQS1_C	IO_L15N_XCC_N5P1_M0P85_701	1.2
AL39	DDR4_0_DQS1_T	IO_L15P_XCC_N5P0_M0P84_701	1.2
AG46	DDR4_0_DQS2_C	IO_L3N_XCC_N1P1_M0P7_700	1.2
AH46	DDR4_0_DQS2_T	IO_L3P_XCC_N1P0_M0P6_700	1.2
AG45	DDR4_0_DQS3_C	IO_L9N_GC_XCC_N3P1_M0P19_700	1.2
AH45	DDR4_0_DQS3_T	IO_L9P_GC_XCC_N3P0_M0P18_700	1.2
AN45	DDR4_0_DQS4_C	IO_L3N_XCC_N1P1_M0P61_701	1.2
AP45	DDR4_0_DQS4_T	IO_L3P_XCC_N1P0_M0P60_701	1.2
AT46	DDR4_0_DQS5_C	IO_L6N_GC_XCC_N2P1_M0P67_701	1.2
AR46	DDR4_0_DQS5_T	IO_L6P_GC_XCC_N2P0_M0P66_701	1.2
BA46	DDR4_0_DQS6_C	IO_L0N_XCC_N0P1_M0P109_702	1.2
AY47	DDR4_0_DQS6_T	IO_L0P_XCC_N0P0_M0P108_702	1.2
BB45	DDR4_0_DQS7_C	IO_L9N_GC_XCC_N3P1_M0P127_702	1.2
BB44	DDR4_0_DQS7_T	IO_L9P_GC_XCC_N3P0_M0P126_702	1.2
BA42	DDR4_0_DQS8_C	IO_L15N_XCC_N5P1_M0P139_702	1.2
BB43	DDR4_0_DQS8_T	IO_L15P_XCC_N5P0_M0P138_702	1.2
AD39	DDR4_0_ODT	IO_L23N_N7P5_M0P47_700	1.2
AD40	DDR4_0_PARITY	IO_L13N_N4P3_M0P27_700	1.2
AD37	DDR4_0_RAS_N	IO_L19N_N6P3_M0P39_700	1.2
AK42	DDR4_0_RESET_N	IO_L25P_N8P2_M0P104_701	1.2
BE27	DDR4_1_A0	IO_L3P_XCC_N1P0_M1P114_705	1.2

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
BC26	DDR4_1_A1	IO_L8N_N2P5_M1P125_705	1.2
BG28	DDR4_1_A10	IO_L0N_XCC_N0P1_M1P109_705	1.2
AV29	DDR4_1_A11	IO_L25P_N8P2_M1P158_705	1.2
AP27	DDR4_1_A12	IO_L21N_XCC_N7P1_M1P151_705	1.2
AY27	DDR4_1_A13	IO_L24N_GC_XCC_N8P1_M1P157_705	1.2
BB28	DDR4_1_A14	IO_L7N_N2P3_M1P123_705	1.2
BD29	DDR4_1_A15	IO_L11N_N3P5_M1P131_705	1.2
BB26	DDR4_1_A2	IO_L8P_N2P4_M1P124_705	1.2
BG30	DDR4_1_A3	IO_L5P_N1P4_M1P118_705	1.2
BD27	DDR4_1_A4	IO_L9P_GC_XCC_N3P0_M1P126_705	1.2
AW25	DDR4_1_A5	IO_L26P_N8P4_M1P160_705	1.2
AW27	DDR4_1_A6	IO_L24P_GC_XCC_N8P0_M1P156_705	1.2
AU27	DDR4_1_A7	IO_L15N_XCC_N5P1_M1P139_705	1.2
AW28	DDR4_1_A8	IO_L25N_N8P3_M1P159_705	1.2
BF26	DDR4_1_A9	IO_L4P_N1P2_M1P116_705	1.2
BF28	DDR4_1_ACT_N	IO_L3N_XCC_N1P1_M1P115_705	1.2
BA32	DDR4_1_ALERT_N	IO_L25N_N8P3_M1P105_704	1.2
BG29	DDR4_1_BA0	IO_L5N_N1P5_M1P119_705	1.2
BC27	DDR4_1_BA1	IO_L9N_GC_XCC_N3P1_M1P127_705	1.2
BF29	DDR4_1_BG0	IO_L0P_XCC_N0P0_M1P108_705	1.2
BE26	DDR4_1_CKE	IO_L2P_N0P4_M1P112_705	1.2
BD28	DDR4_1_CLK_C	IO_L6N_GC_XCC_N2P1_M1P121_705	1.2
BC28	DDR4_1_CLK_T	IO_L6P_GC_XCC_N2P0_M1P120_705	1.2
BD30	DDR4_1_CS_N	IO_L11P_N3P4_M1P130_705	1.2
AW31	DDR4_1_DEBUG	IO_L26P_N8P4_M1P106_704	1.2
AV26	DDR4_1_DM0	IO_L15P_XCC_N5P0_M1P138_705	1.2
AR26	DDR4_1_DM1	IO_L21P_XCC_N7P0_M1P150_705	1.2
AR33	DDR4_1_DM2	IO_L12P_GC_XCC_N4P0_M1P78_704	1.2
AR30	DDR4_1_DM3	IO_L21P_XCC_N7P0_M1P96_704	1.2
BE31	DDR4_1_DM4	IO_L9P_GC_XCC_N3P0_M1P72_704	1.2
BD33	DDR4_1_DM5	IO_L3P_XCC_N1P0_M1P60_704	1.2
BD37	DDR4_1_DM6	IO_L9P_GC_XCC_N3P0_M1P18_703	1.2
AW36	DDR4_1_DM7	IO_L15P_XCC_N5P0_M1P30_703	1.2
AT38	DDR4_1_DM8	IO_L18P_XCC_N6P0_M1P36_703	1.2
AT29	DDR4_1_DQ0	IO_L13P_N4P2_M1P134_705	1.2
AU25	DDR4_1_DQ1	IO_L16P_N5P2_M1P140_705	1.2

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
AP25	DDR4_1_DQ10	IO_L22N_N7P3_M1P153_705	1.2
AM27	DDR4_1_DQ11	IO_L23P_N7P4_M1P154_705	1.2
AM26	DDR4_1_DQ12	IO_L20P_N6P4_M1P148_705	1.2
AM29	DDR4_1_DQ13	IO_L19P_N6P2_M1P146_705	1.2
AN25	DDR4_1_DQ14	IO_L22P_N7P2_M1P152_705	1.2
AN28	DDR4_1_DQ15	IO_L23N_N7P5_M1P155_705	1.2
AP34	DDR4_1_DQ16	IO_L13N_N4P3_M1P81_704	1.2
AU33	DDR4_1_DQ17	IO_L14P_N4P4_M1P82_704	1.2
AR32	DDR4_1_DQ18	IO_L17N_N5P5_M1P89_704	1.2
AV33	DDR4_1_DQ19	IO_L16P_N5P2_M1P86_704	1.2
AT28	DDR4_1_DQ2	IO_L17N_N5P5_M1P143_705	1.2
AN34	DDR4_1_DQ20	IO_L13P_N4P2_M1P80_704	1.2
AV34	DDR4_1_DQ21	IO_L14N_N4P5_M1P83_704	1.2
AP33	DDR4_1_DQ22	IO_L17P_N5P4_M1P88_704	1.2
AW33	DDR4_1_DQ23	IO_L16N_N5P3_M1P87_704	1.2
AV31	DDR4_1_DQ24	IO_L20P_N6P4_M1P94_704	1.2
AM33	DDR4_1_DQ25	IO_L19P_N6P2_M1P92_704	1.2
AV30	DDR4_1_DQ26	IO_L20N_N6P5_M1P95_704	1.2
AN31	DDR4_1_DQ27	IO_L23N_N7P5_M1P101_704	1.2
AT31	DDR4_1_DQ28	IO_L22P_N7P2_M1P98_704	1.2
AM30	DDR4_1_DQ29	IO_L23P_N7P4_M1P100_704	1.2
AT26	DDR4_1_DQ3	IO_L14P_N4P4_M1P136_705	1.2
AU31	DDR4_1_DQ30	IO_L22N_N7P3_M1P99_704	1.2
AM32	DDR4_1_DQ31	IO_L19N_N6P3_M1P93_704	1.2
BF31	DDR4_1_DQ32	IO_L10P_N3P2_M1P74_704	1.2
BE32	DDR4_1_DQ33	IO_L8P_N2P4_M1P70_704	1.2
BF32	DDR4_1_DQ34	IO_L8N_N2P5_M1P71_704	1.2
BC32	DDR4_1_DQ35	IO_L11N_N3P5_M1P77_704	1.2
BB30	DDR4_1_DQ36	IO_L7N_N2P3_M1P69_704	1.2
BB33	DDR4_1_DQ37	IO_L11P_N3P4_M1P76_704	1.2
BG31	DDR4_1_DQ38	IO_L10N_N3P3_M1P75_704	1.2
BB31	DDR4_1_DQ39	IO_L7P_N2P2_M1P68_704	1.2
AR29	DDR4_1_DQ4	IO_L17P_N5P4_M1P142_705	1.2
BC33	DDR4_1_DQ40	IO_L4N_N1P3_M1P63_704	1.2
BE35	DDR4_1_DQ41	IO_L1P_N0P2_M1P56_704	1.2
BD34	DDR4_1_DQ42	IO_L2N_N0P5_M1P59_704	1.2

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
BF34	DDR4_1_DQ43	IO_L1N_N0P3_M1P57_704	1.2
BB34	DDR4_1_DQ44	IO_L4P_N1P2_M1P62_704	1.2
BG35	DDR4_1_DQ45	IO_L5P_N1P4_M1P64_704	1.2
BD35	DDR4_1_DQ46	IO_L2P_N0P4_M1P58_704	1.2
BG34	DDR4_1_DQ47	IO_L5N_N1P5_M1P65_704	1.2
BB35	DDR4_1_DQ48	IO_L10P_N3P2_M1P20_703	1.2
BD40	DDR4_1_DQ49	IO_L7N_N2P3_M1P15_703	1.2
AV25	DDR4_1_DQ5	IO_L16N_N5P3_M1P141_705	1.2
BB36	DDR4_1_DQ50	IO_L8P_N2P4_M1P16_703	1.2
BC38	DDR4_1_DQ51	IO_L11N_N3P5_M1P23_703	1.2
BC35	DDR4_1_DQ52	IO_L10N_N3P3_M1P21_703	1.2
BB38	DDR4_1_DQ53	IO_L11P_N3P4_M1P22_703	1.2
BC36	DDR4_1_DQ54	IO_L8N_N2P5_M1P17_703	1.2
BC40	DDR4_1_DQ55	IO_L7P_N2P2_M1P14_703	1.2
AV35	DDR4_1_DQ56	IO_L16N_N5P3_M1P33_703	1.2
AU36	DDR4_1_DQ57	IO_L17N_N5P5_M1P35_703	1.2
AW35	DDR4_1_DQ58	IO_L14P_N4P4_M1P28_703	1.2
AY39	DDR4_1_DQ59	IO_L13N_N4P3_M1P27_703	1.2
AU29	DDR4_1_DQ6	IO_L13N_N4P3_M1P135_705	1.2
AU35	DDR4_1_DQ60	IO_L16P_N5P2_M1P32_703	1.2
AU37	DDR4_1_DQ61	IO_L17P_N5P4_M1P34_703	1.2
AY35	DDR4_1_DQ62	IO_L14N_N4P5_M1P29_703	1.2
AW39	DDR4_1_DQ63	IO_L13P_N4P2_M1P26_703	1.2
AR35	DDR4_1_DQ64	IO_L20P_N6P4_M1P40_703	1.2
AR37	DDR4_1_DQ65	IO_L23N_N7P5_M1P47_703	1.2
AM35	DDR4_1_DQ66	IO_L19N_N6P3_M1P39_703	1.2
AP36	DDR4_1_DQ67	IO_L22N_N7P3_M1P45_703	1.2
AN35	DDR4_1_DQ68	IO_L22P_N7P2_M1P44_703	1.2
AM36	DDR4_1_DQ69	IO_L19P_N6P2_M1P38_703	1.2
AT25	DDR4_1_DQ7	IO_L14N_N4P5_M1P137_705	1.2
AT35	DDR4_1_DQ70	IO_L20N_N6P5_M1P41_703	1.2
AP38	DDR4_1_DQ71	IO_L23P_N7P4_M1P46_703	1.2
AN26	DDR4_1_DQ8	IO_L20N_N6P5_M1P149_705	1.2
AN29	DDR4_1_DQ9	IO_L19N_N6P3_M1P147_705	1.2
AV27	DDR4_1_DQS0_C	IO_L12N_GC_XCC_N4P1_M1P133_705	1.2
AU28	DDR4_1_DQS0_T	IO_L12P_GC_XCC_N4P0_M1P132_705	1.2

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
AR27	DDR4_1_DQS1_C	IO_L18N_XCC_N6P1_M1P145_705	1.2
AP28	DDR4_1_DQS1_T	IO_L18P_XCC_N6P0_M1P144_705	1.2
AT32	DDR4_1_DQS2_C	IO_L15N_XCC_N5P1_M1P85_704	1.2
AU32	DDR4_1_DQS2_T	IO_L15P_XCC_N5P0_M1P84_704	1.2
AP31	DDR4_1_DQS3_C	IO_L18N_XCC_N6P1_M1P91_704	1.2
AN32	DDR4_1_DQS3_T	IO_L18P_XCC_N6P0_M1P90_704	1.2
BC30	DDR4_1_DQS4_C	IO_L6N_GC_XCC_N2P1_M1P67_704	1.2
BC31	DDR4_1_DQS4_T	IO_L6P_GC_XCC_N2P0_M1P66_704	1.2
BG33	DDR4_1_DQS5_C	IO_L0N_XCC_N0P1_M1P55_704	1.2
BF33	DDR4_1_DQS5_T	IO_L0P_XCC_N0P0_M1P54_704	1.2
BD38	DDR4_1_DQS6_C	IO_L6N_GC_XCC_N2P1_M1P13_703	1.2
BD39	DDR4_1_DQS6_T	IO_L6P_GC_XCC_N2P0_M1P12_703	1.2
AW37	DDR4_1_DQS7_C	IO_L12N_GC_XCC_N4P1_M1P25_703	1.2
AV38	DDR4_1_DQS7_T	IO_L12P_GC_XCC_N4P0_M1P24_703	1.2
AP37	DDR4_1_DQS8_C	IO_L21N_XCC_N7P1_M1P43_703	1.2
AR36	DDR4_1_DQS8_T	IO_L21P_XCC_N7P0_M1P42_703	1.2
BF27	DDR4_1_ODT	IO_L2N_N0P5_M1P113_705	1.2
BA27	DDR4_1_PARITY	IO_L10N_N3P3_M1P129_705	1.2
BG26	DDR4_1_RAS_N	IO_L4N_N1P3_M1P117_705	1.2
BA33	DDR4_1_RESET_N	IO_L25P_N8P2_M1P104_704	1.2
AF6	DP0_C2M_N	GTY_TXN0_200	MGT
AF7	DP0_C2M_P	GTY_TXP0_200	MGT
AF1	DP0_M2C_N	GTY_RXN0_200	MGT
AF2	DP0_M2C_P	GTY_RXP0_200	MGT
AE8	DP1_C2M_N	GTY_TXN1_200	MGT
AE9	DP1_C2M_P	GTY_TXP1_200	MGT
AE3	DP1_M2C_N	GTY_RXN1_200	MGT
AE4	DP1_M2C_P	GTY_RXP1_200	MGT
T6	DP10_C2M_N	GTY_TXN2_202	MGT
T7	DP10_C2M_P	GTY_TXP2_202	MGT
T1	DP10_M2C_N	GTY_RXN2_202	MGT
T2	DP10_M2C_P	GTY_RXP2_202	MGT
R8	DP11_C2M_N	GTY_TXN3_202	MGT
R9	DP11_C2M_P	GTY_TXP3_202	MGT
R3	DP11_M2C_N	GTY_RXN3_202	MGT
R4	DP11_M2C_P	GTY_RXP3_202	MGT

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
P6	DP12_C2M_N	GTY_TXN0_203	MGT
P7	DP12_C2M_P	GTY_TXP0_203	MGT
P1	DP12_M2C_N	GTY_RXN0_203	MGT
P2	DP12_M2C_P	GTY_RXP0_203	MGT
N8	DP13_C2M_N	GTY_TXN1_203	MGT
N9	DP13_C2M_P	GTY_TXP1_203	MGT
N3	DP13_M2C_N	GTY_RXN1_203	MGT
N4	DP13_M2C_P	GTY_RXP1_203	MGT
M6	DP14_C2M_N	GTY_TXN2_203	MGT
M7	DP14_C2M_P	GTY_TXP2_203	MGT
M1	DP14_M2C_N	GTY_RXN2_203	MGT
M2	DP14_M2C_P	GTY_RXP2_203	MGT
L8	DP15_C2M_N	GTY_TXN3_203	MGT
L9	DP15_C2M_P	GTY_TXP3_203	MGT
L3	DP15_M2C_N	GTY_RXN3_203	MGT
L4	DP15_M2C_P	GTY_RXP3_203	MGT
K6	DP16_C2M_N	GTY_TXN0_204	MGT
K7	DP16_C2M_P	GTY_TXP0_204	MGT
K1	DP16_M2C_N	GTY_RXN0_204	MGT
K2	DP16_M2C_P	GTY_RXP0_204	MGT
K10	DP17_C2M_N	GTY_TXN1_204	MGT
K11	DP17_C2M_P	GTY_TXP1_204	MGT
J3	DP17_M2C_N	GTY_RXN1_204	MGT
J4	DP17_M2C_P	GTY_RXP1_204	MGT
J8	DP18_C2M_N	GTY_TXN2_204	MGT
J9	DP18_C2M_P	GTY_TXP2_204	MGT
H1	DP18_M2C_N	GTY_RXN2_204	MGT
H2	DP18_M2C_P	GTY_RXP2_204	MGT
H10	DP19_C2M_N	GTY_TXN3_204	MGT
H11	DP19_C2M_P	GTY_TXP3_204	MGT
H5	DP19_M2C_N	GTY_RXN3_204	MGT
H6	DP19_M2C_P	GTY_RXP3_204	MGT
AD6	DP2_C2M_N	GTY_TXN2_200	MGT
AD7	DP2_C2M_P	GTY_TXP2_200	MGT
AD1	DP2_M2C_N	GTY_RXN2_200	MGT
AD2	DP2_M2C_P	GTY_RXP2_200	MGT

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
G8	DP20_C2M_N	GTY_TXN0_205	MGT
G9	DP20_C2M_P	GTY_TXP0_205	MGT
G3	DP20_M2C_N	GTY_RXN0_205	MGT
G4	DP20_M2C_P	GTY_RXP0_205	MGT
F10	DP21_C2M_N	GTY_TXN1_205	MGT
F11	DP21_C2M_P	GTY_TXP1_205	MGT
F1	DP21_M2C_N	GTY_RXN1_205	MGT
F2	DP21_M2C_P	GTY_RXP1_205	MGT
E8	DP22_C2M_N	GTY_TXN2_205	MGT
E9	DP22_C2M_P	GTY_TXP2_205	MGT
F5	DP22_M2C_N	GTY_RXN2_205	MGT
F6	DP22_M2C_P	GTY_RXP2_205	MGT
D10	DP23_C2M_N	GTY_TXN3_205	MGT
D11	DP23_C2M_P	GTY_TXP3_205	MGT
E3	DP23_M2C_N	GTY_RXN3_205	MGT
E4	DP23_M2C_P	GTY_RXP3_205	MGT
AC8	DP3_C2M_N	GTY_TXN3_200	MGT
AC9	DP3_C2M_P	GTY_TXP3_200	MGT
AC3	DP3_M2C_N	GTY_RXN3_200	MGT
AC4	DP3_M2C_P	GTY_RXP3_200	MGT
AB6	DP4_C2M_N	GTY_TXN0_201	MGT
AB7	DP4_C2M_P	GTY_TXP0_201	MGT
AB1	DP4_M2C_N	GTY_RXN0_201	MGT
AB2	DP4_M2C_P	GTY_RXP0_201	MGT
AA8	DP5_C2M_N	GTY_TXN1_201	MGT
AA9	DP5_C2M_P	GTY_TXP1_201	MGT
AA3	DP5_M2C_N	GTY_RXN1_201	MGT
AA4	DP5_M2C_P	GTY_RXP1_201	MGT
Y6	DP6_C2M_N	GTY_TXN2_201	MGT
Y7	DP6_C2M_P	GTY_TXP2_201	MGT
Y1	DP6_M2C_N	GTY_RXN2_201	MGT
Y2	DP6_M2C_P	GTY_RXP2_201	MGT
W8	DP7_C2M_N	GTY_TXN3_201	MGT
W9	DP7_C2M_P	GTY_TXP3_201	MGT
W3	DP7_M2C_N	GTY_RXN3_201	MGT
W4	DP7_M2C_P	GTY_RXP3_201	MGT

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
V6	DP8_C2M_N	GTY_TXN0_202	MGT
V7	DP8_C2M_P	GTY_TXP0_202	MGT
V1	DP8_M2C_N	GTY_RXN0_202	MGT
V2	DP8_M2C_P	GTY_RXP0_202	MGT
U8	DP9_C2M_N	GTY_TXN1_202	MGT
U9	DP9_C2M_P	GTY_TXP1_202	MGT
U3	DP9_M2C_N	GTY_RXN1_202	MGT
U4	DP9_M2C_P	GTY_RXP1_202	MGT
G19*	EN_VCC_INT_MIO (Rev3-)	PMC_MIO40_501	1.8
A32	ERROR_OUT	ERROR_OUT_503	1.5
AR1	FABRIC_CLK_PIN_N	IO_L9N_GC_XCC_N3P1_M3P73_710	1.5
AR2	FABRIC_CLK_PIN_P	IO_L9P_GC_XCC_N3P0_M3P72_710	1.5
L37	FAN_FAIL_1V8_L	IO_L0N_306	1.8
C12	FIREFLY_CLK_PIN_N	GTY_REFCLKN0_206	MGT REFCLK
C13	FIREFLY_CLK_PIN_P	GTY_REFCLKP0_206	MGT REFCLK
H17	FIREFLY_INT_L	IO_L7P_406	3.3
J19	FIREFLY_MODPRS_L	IO_L6N_406	3.3
H18	FIREFLY_RST_ L	IO_L7N_406	3.3
D1	FIREFLY_RX0_N	GTY_RXN0_206	MGT
D2	FIREFLY_RX0_P	GTY_RXP0_206	MGT
D5	FIREFLY_RX1_N	GTY_RXN1_206	MGT
D6	FIREFLY_RX1_P	GTY_RXP1_206	MGT
C3	FIREFLY_RX2_N	GTY_RXN2_206	MGT
C4	FIREFLY_RX2_P	GTY_RXP2_206	MGT
B5	FIREFLY_RX3_N	GTY_RXN3_206	MGT
B6	FIREFLY_RX3_P	GTY_RXP3_206	MGT
J21	FIREFLY_SCL	IO_L8N_406	3.3
J20	FIREFLY_SDA	IO_L8P_406	3.3
C8	FIREFLY_TX0_N	GTY_TXN0_206	MGT
C9	FIREFLY_TX0_P	GTY_TXP0_206	MGT
B10	FIREFLY_TX1_N	GTY_TXN1_206	MGT
B11	FIREFLY_TX1_P	GTY_TXP1_206	MGT
A8	FIREFLY_TX2_N	GTY_TXN2_206	MGT
A9	FIREFLY_TX2_P	GTY_TXP2_206	MGT
A12	FIREFLY_TX3_N	GTY_TXN3_206	MGT
A13	FIREFLY_TX3_P	GTY_TXP3_206	MGT

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
C18	FPGA_SYSMON_I2C_SCL	PMC_MIO44_501	1.8
A18	FPGA_SYSMON_I2C_SDA	PMC_MIO45_501	1.8
K14	GBTCLK2_PIN_N	GTY_REFCLKN1_202	MGT REFCLK
K15	GBTCLK2_PIN_P	GTY_REFCLKP1_202	MGT REFCLK
H14	GBTCLK3_PIN_N	GTY_REFCLKN1_203	MGT REFCLK
H15	GBTCLK3_PIN_P	GTY_REFCLKP1_203	MGT REFCLK
D14	GBTCLK5_PIN_N	GTY_REFCLKN1_205	MGT REFCLK
D15	GBTCLK5_PIN_P	GTY_REFCLKP1_205	MGT REFCLK
C33	GEM0_MDC	LPD_MIO24_502	3.3
D33	GEM0_MDIO	LPD_MIO25_502	3.3
C19	GEM0_RST_L	PMC_MIO37_501	1.8
B37	GEM0_RX_CLK	LPD_MIO6_502	3.3
D36	GEM0_RX_CTRL	LPD_MIO11_502	3.3
C37	GEM0_RXD_0	LPD_MIO7_502	3.3
E37	GEM0_RXD_1	LPD_MIO8_502	3.3
F37	GEM0_RXD_2	LPD_MIO9_502	3.3
E36	GEM0_RXD_3	LPD_MIO10_502	3.3
A39	GEM0_TX_CLK	LPD_MIO0_502	3.3
A37	GEM0_TX_CTRL	LPD_MIO5_502	3.3
B39	GEM0_TXD_0	LPD_MIO1_502	3.3
C39	GEM0_TXD_1	LPD_MIO2_502	3.3
C38	GEM0_TXD_2	LPD_MIO3_502	3.3
A38	GEM0_TXD_3	LPD_MIO4_502	3.3
AV13	HA00_CC_N	IO_L12N_GC_XCC_N4P1_M2P133_708	FMC_VADJ
AU13	HA00_CC_P	IO_L12P_GC_XCC_N4P0_M2P132_708	FMC_VADJ
BD13	HA01_CC_N	IO_L9N_GC_XCC_N3P1_M2P127_708	FMC_VADJ
BC13	HA01_CC_P	IO_L9P_GC_XCC_N3P0_M2P126_708	FMC_VADJ
AU15	HA02_N	IO_L13N_N4P3_M2P135_708	FMC_VADJ
AT14	HA02_P	IO_L13P_N4P2_M2P134_708	FMC_VADJ
AN13	HA03_N	IO_L21N_XCC_N7P1_M2P151_708	FMC_VADJ
AP12	HA03_P	IO_L21P_XCC_N7P0_M2P150_708	FMC_VADJ
AT11	HA04_N	IO_L22N_N7P3_M2P153_708	FMC_VADJ
AR11	HA04_P	IO_L22P_N7P2_M2P152_708	FMC_VADJ
AR12	HA05_N	IO_L20N_N6P5_M2P149_708	FMC_VADJ
AP11	HA05_P	IO_L20P_N6P4_M2P148_708	FMC_VADJ
AT13	HA06_N	IO_L18N_XCC_N6P1_M2P145_708	FMC_VADJ

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
AR14	HA06_P	IO_L18P_XCC_N6P0_M2P144_708	FMC_VADJ
AU11	HA07_N	IO_L14N_N4P5_M2P137_708	FMC_VADJ
AU12	HA07_P	IO_L14P_N4P4_M2P136_708	FMC_VADJ
AR15	HA08_N	IO_L19N_N6P3_M2P147_708	FMC_VADJ
AP15	HA08_P	IO_L19P_N6P2_M2P146_708	FMC_VADJ
AP13	HA09_N	IO_L23N_N7P5_M2P155_708	FMC_VADJ
AN14	HA09_P	IO_L23P_N7P4_M2P154_708	FMC_VADJ
AV14	HA10_N	IO_L17N_N5P5_M2P143_708	FMC_VADJ
AV15	HA10_P	IO_L17P_N5P4_M2P142_708	FMC_VADJ
BC11	HA11_N	IO_L10N_N3P3_M2P129_708	FMC_VADJ
BB11	HA11_P	IO_L10P_N3P2_M2P128_708	FMC_VADJ
AW13	HA12_N	IO_L15N_XCC_N5P1_M2P139_708	FMC_VADJ
AW12	HA12_P	IO_L15P_XCC_N5P0_M2P138_708	FMC_VADJ
AW11	HA13_N	IO_L16N_N5P3_M2P141_708	FMC_VADJ
AV11	HA13_P	IO_L16P_N5P2_M2P140_708	FMC_VADJ
BF12	HA14_N	IO_L2N_N0P5_M2P113_708	FMC_VADJ
BE11	HA14_P	IO_L2P_N0P4_M2P112_708	FMC_VADJ
BE14	HA15_N	IO_L1N_N0P3_M2P111_708	FMC_VADJ
BE15	HA15_P	IO_L1P_N0P2_M2P110_708	FMC_VADJ
BD12	HA16_N	IO_L8N_N2P5_M2P125_708	FMC_VADJ
BC12	HA16_P	IO_L8P_N2P4_M2P124_708	FMC_VADJ
BB13	HA17_CC_N	IO_L6N_GC_XCC_N2P1_M2P121_708	FMC_VADJ
BB14	HA17_CC_P	IO_L6P_GC_XCC_N2P0_M2P120_708	FMC_VADJ
BC15	HA18_N	IO_L7N_N2P3_M2P123_708	FMC_VADJ
BB15	HA18_P	IO_L7P_N2P2_M2P122_708	FMC_VADJ
BD14	HA19_N	IO_L11N_N3P5_M2P131_708	FMC_VADJ
BD15	HA19_P	IO_L11P_N3P4_M2P130_708	FMC_VADJ
BG11	HA20_N	IO_L4N_N1P3_M2P117_708	FMC_VADJ
BF11	HA20_P	IO_L4P_N1P2_M2P116_708	FMC_VADJ
BF13	HA21_N	IO_L3N_XCC_N1P1_M2P115_708	FMC_VADJ
BE12	HA21_P	IO_L3P_XCC_N1P0_M2P114_708	FMC_VADJ
BG13	HA22_N	IO_L0N_XCC_N0P1_M2P109_708	FMC_VADJ
BF14	HA22_P	IO_L0P_XCC_N0P0_M2P108_708	FMC_VADJ
BG14	HA23_N	IO_L5N_N1P5_M2P119_708	FMC_VADJ
BG15	HA23_P	IO_L5P_N1P4_M2P118_708	FMC_VADJ
BB4	HB00_CC_N	IO_L9N_GC_XCC_N3P1_M3P19_709	FMC_VADJ

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
BB3	HB00_CC_P	IO_L9P_GC_XCC_N3P0_M3P18_709	FMC_VADJ
AY1	HB01_N	IO_L4N_N1P3_M3P9_709	FMC_VADJ
AY2	HB01_P	IO_L4P_N1P2_M3P8_709	FMC_VADJ
BA2	HB02_N	IO_L2N_N0P5_M3P5_709	FMC_VADJ
BA3	HB02_P	IO_L2P_N0P4_M3P4_709	FMC_VADJ
AY4	HB03_N	IO_L10N_N3P3_M3P21_709	FMC_VADJ
AY5	HB03_P	IO_L10P_N3P2_M3P20_709	FMC_VADJ
BB1	HB04_N	IO_L3N_XCC_N1P1_M3P7_709	FMC_VADJ
BA1	HB04_P	IO_L3P_XCC_N1P0_M3P6_709	FMC_VADJ
BA4	HB05_N	IO_L8N_N2P5_M3P17_709	FMC_VADJ
BB5	HB05_P	IO_L8P_N2P4_M3P16_709	FMC_VADJ
BC3	HB06_CC_N	IO_L6N_GC_XCC_N2P1_M3P13_709	FMC_VADJ
BD4	HB06_CC_P	IO_L6P_GC_XCC_N2P0_M3P12_709	FMC_VADJ
BD9	HB07_N	IO_L21N_XCC_N7P1_M3P43_709	FMC_VADJ
BD10	HB07_P	IO_L21P_XCC_N7P0_M3P42_709	FMC_VADJ
BE4	HB08_N	IO_L11N_N3P5_M3P23_709	FMC_VADJ
BF4	HB08_P	IO_L11P_N3P4_M3P22_709	FMC_VADJ
BD2	HB09_N	IO_L5N_N1P5_M3P11_709	FMC_VADJ
BD3	HB09_P	IO_L5P_N1P4_M3P10_709	FMC_VADJ
BC1	HB10_N	IO_L0N_XCC_N0P1_M3P1_709	FMC_VADJ
BC2	HB10_P	IO_L0P_XCC_N0P0_M3P0_709	FMC_VADJ
BE10	HB11_N	IO_L18N_XCC_N6P1_M3P37_709	FMC_VADJ
BE9	HB11_P	IO_L18P_XCC_N6P0_M3P36_709	FMC_VADJ
AY6	HB12_N	IO_L16N_N5P3_M3P33_709	FMC_VADJ
AY7	HB12_P	IO_L16P_N5P2_M3P32_709	FMC_VADJ
BB9	HB13_N	IO_L20N_N6P5_M3P41_709	FMC_VADJ
BC10	HB13_P	IO_L20P_N6P4_M3P40_709	FMC_VADJ
BG4	HB14_N	IO_L7N_N2P3_M3P15_709	FMC_VADJ
BG5	HB14_P	IO_L7P_N2P2_M3P14_709	FMC_VADJ
BE2	HB15_N	IO_L1N_N0P3_M3P3_709	FMC_VADJ
BF3	HB15_P	IO_L1P_N0P2_M3P2_709	FMC_VADJ
BC7	HB16_N	IO_L15N_XCC_N5P1_M3P31_709	FMC_VADJ
BC8	HB16_P	IO_L15P_XCC_N5P0_M3P30_709	FMC_VADJ
BC6	HB17_CC_N	IO_L12N_GC_XCC_N4P1_M3P25_709	FMC_VADJ
BD7	HB17_CC_P	IO_L12P_GC_XCC_N4P0_M3P24_709	FMC_VADJ
BG8	HB18_N	IO_L19N_N6P3_M3P39_709	FMC_VADJ

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
BG9	HB18_P	IO_L19P_N6P2_M3P38_709	FMC_VADJ
BA8	HB19_N	IO_L14N_N4P5_M3P29_709	FMC_VADJ
BB8	HB19_P	IO_L14P_N4P4_M3P28_709	FMC_VADJ
BF7	HB20_N	IO_L13N_N4P3_M3P27_709	FMC_VADJ
BF8	HB20_P	IO_L13P_N4P2_M3P26_709	FMC_VADJ
BE7	HB21_N	IO_L17N_N5P5_M3P35_709	FMC_VADJ
BD8	HB21_P	IO_L17P_N5P4_M3P34_709	FMC_VADJ
AY18	LA00_CC_N	IO_L24N_GC_XCC_N8P1_M2P103_707	FMC_VADJ
AW19	LA00_CC_P	IO_L24P_GC_XCC_N8P0_M2P102_707	FMC_VADJ
AP18	LA01_CC_N	IO_L12N_GC_XCC_N4P1_M2P79_707	FMC_VADJ
AP19	LA01_CC_P	IO_L12P_GC_XCC_N4P0_M2P78_707	FMC_VADJ
AM20	LA02_N	IO_L13N_N4P3_M2P81_707	FMC_VADJ
AM21	LA02_P	IO_L13P_N4P2_M2P80_707	FMC_VADJ
AN19	LA03_N	IO_L17N_N5P5_M2P89_707	FMC_VADJ
AN20	LA03_P	IO_L17P_N5P4_M2P88_707	FMC_VADJ
BG19	LA04_N	IO_L2N_N0P5_M2P59_707	FMC_VADJ
BF19	LA04_P	IO_L2P_N0P4_M2P58_707	FMC_VADJ
AM17	LA05_N	IO_L23N_N7P5_M2P101_707	FMC_VADJ
AL16	LA05_P	IO_L23P_N7P4_M2P100_707	FMC_VADJ
AR20	LA06_N	IO_L15N_XCC_N5P1_M2P85_707	FMC_VADJ
AT20	LA06_P	IO_L15P_XCC_N5P0_M2P84_707	FMC_VADJ
AV18	LA07_N	IO_L26N_N8P5_M2P107_707	FMC_VADJ
AV19	LA07_P	IO_L26P_N8P4_M2P106_707	FMC_VADJ
AU16	LA08_N	IO_L22N_N7P3_M2P99_707	FMC_VADJ
AT17	LA08_P	IO_L22P_N7P2_M2P98_707	FMC_VADJ
AN17	LA09_N	IO_L19N_N6P3_M2P93_707	FMC_VADJ
AM18	LA09_P	IO_L19P_N6P2_M2P92_707	FMC_VADJ
AR17	LA10_N	IO_L18N_XCC_N6P1_M2P91_707	FMC_VADJ
AT16	LA10_P	IO_L18P_XCC_N6P0_M2P90_707	FMC_VADJ
AP16	LA11_N	IO_L21N_XCC_N7P1_M2P97_707	FMC_VADJ
AN16	LA11_P	IO_L21P_XCC_N7P0_M2P96_707	FMC_VADJ
AT19	LA12_N	IO_L14N_N4P5_M2P83_707	FMC_VADJ
AR18	LA12_P	IO_L14P_N4P4_M2P82_707	FMC_VADJ
AU19	LA13_N	IO_L16N_N5P3_M2P87_707	FMC_VADJ
AU20	LA13_P	IO_L16P_N5P2_M2P86_707	FMC_VADJ
AV17	LA14_N	IO_L20N_N6P5_M2P95_707	FMC_VADJ

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
AU17	LA14_P	IO_L20P_N6P4_M2P94_707	FMC_VADJ
BB19	LA15_N	IO_L1N_N0P3_M2P57_707	FMC_VADJ
BB20	LA15_P	IO_L1P_N0P2_M2P56_707	FMC_VADJ
AY19	LA16_N	IO_L25N_N8P3_M2P105_707	FMC_VADJ
AW20	LA16_P	IO_L25P_N8P2_M2P104_707	FMC_VADJ
BC16	LA17_CC_N	IO_L6N_GC_XCC_N2P1_M2P67_707	FMC_VADJ
BB16	LA17_CC_P	IO_L6P_GC_XCC_N2P0_M2P66_707	FMC_VADJ
BD17	LA18_CC_N	IO_L9N_GC_XCC_N3P1_M2P73_707	FMC_VADJ
BE17	LA18_CC_P	IO_L9P_GC_XCC_N3P0_M2P72_707	FMC_VADJ
BA16	LA19_N	IO_L7N_N2P3_M2P69_707	FMC_VADJ
BA17	LA19_P	IO_L7P_N2P2_M2P68_707	FMC_VADJ
BA19	LA20_N	IO_L5N_N1P5_M2P65_707	FMC_VADJ
BA20	LA20_P	IO_L5P_N1P4_M2P64_707	FMC_VADJ
BD19	LA21_N	IO_L0N_XCC_N0P1_M2P55_707	FMC_VADJ
BE19	LA21_P	IO_L0P_XCC_N0P0_M2P54_707	FMC_VADJ
BC17	LA22_N	IO_L11N_N3P5_M2P77_707	FMC_VADJ
BB18	LA22_P	IO_L11P_N3P4_M2P76_707	FMC_VADJ
BD18	LA23_N	IO_L3N_XCC_N1P1_M2P61_707	FMC_VADJ
BC18	LA23_P	IO_L3P_XCC_N1P0_M2P60_707	FMC_VADJ
BG16	LA24_N	IO_L10N_N3P3_M2P75_707	FMC_VADJ
BF16	LA24_P	IO_L10P_N3P2_M2P74_707	FMC_VADJ
BE20	LA25_N	IO_L4N_N1P3_M2P9_706	FMC_VADJ
BE21	LA25_P	IO_L4P_N1P2_M2P8_706	FMC_VADJ
BF17	LA26_N	IO_L8N_N2P5_M2P71_707	FMC_VADJ
BE16	LA26_P	IO_L8P_N2P4_M2P70_707	FMC_VADJ
BE24	LA27_N	IO_L7N_N2P3_M2P15_706	FMC_VADJ
BE25	LA27_P	IO_L7P_N2P2_M2P14_706	FMC_VADJ
BF22	LA28_N	IO_L3N_XCC_N1P1_M2P7_706	FMC_VADJ
BG21	LA28_P	IO_L3P_XCC_N1P0_M2P6_706	FMC_VADJ
BE22	LA29_N	IO_L0N_XCC_N0P1_M2P1_706	FMC_VADJ
BF23	LA29_P	IO_L0P_XCC_N0P0_M2P0_706	FMC_VADJ
BG20	LA30_N	IO_L2N_N0P5_M2P5_706	FMC_VADJ
BF21	LA30_P	IO_L2P_N0P4_M2P4_706	FMC_VADJ
BG18	LA31_N	IO_L4N_N1P3_M2P63_707	FMC_VADJ
BF18	LA31_P	IO_L4P_N1P2_M2P62_707	FMC_VADJ
BG24	LA32_N	IO_L1N_N0P3_M2P3_706	FMC_VADJ

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
BG25	LA32_P	IO_L1P_N0P2_M2P2_706	FMC_VADJ
BG23	LA33_N	IO_L5N_N1P5_M2P11_706	FMC_VADJ
BF24	LA33_P	IO_L5P_N1P4_M2P10_706	FMC_VADJ
C36	LDP_MIO12	LPD_MIO12_502	3.3
B36	LDP_MIO13	LPD_MIO13_502	3.3
A35	LDP_MIO14	LPD_MIO14_502	3.3
B35	LDP_MIO15	LPD_MIO15_502	3.3
D35	LDP_MIO16	LPD_MIO16_502	3.3
E35	LDP_MIO17	LPD_MIO17_502	3.3
F35	LDP_MIO18	LPD_MIO18_502	3.3
G35	LDP_MIO19	LPD_MIO19_502	3.3
D34	LDP_MIO20	LPD_MIO20_502	3.3
C34	LDP_MIO21	LPD_MIO21_502	3.3
B34	LDP_MIO22	LPD_MIO22_502	3.3
A34	LDP_MIO23	LPD_MIO23_502	3.3
C17	LPD_I2C1_SCL_1V8	PMC_MIO48_501	1.8
E17	LPD_I2C1_SDA_1V8	PMC_MIO49_501	1.8
AN43	MEM_CLK_0_PIN_N	IO_L24N_GC_XCC_N8P1_M0P103_701	1.2
AM43	MEM_CLK_0_PIN_P	IO_L24P_GC_XCC_N8P0_M0P102_701	1.2
BA31	MEM_CLK_1_PIN_N	IO_L24N_GC_XCC_N8P1_M1P103_704	1.2
AY31	MEM_CLK_1_PIN_P	IO_L24P_GC_XCC_N8P0_M1P102_704	1.2
AF10	MGT_PROGCLK_0_PIN_N	GTY_REFCLKN0_200	MGT REFCLK
AF11	MGT_PROGCLK_0_PIN_P	GTY_REFCLKP0_200	MGT REFCLK
AB10	MGT_PROGCLK_1_PIN_N	GTY_REFCLKN0_201	MGT REFCLK
AB11	MGT_PROGCLK_1_PIN_P	GTY_REFCLKP0_201	MGT REFCLK
L12	MGT_PROGCLK_2_PIN_N	GTY_REFCLKN0_202	MGT REFCLK
L13	MGT_PROGCLK_2_PIN_P	GTY_REFCLKP0_202	MGT REFCLK
J12	MGT_PROGCLK_3_PIN_N	GTY_REFCLKN0_203	MGT REFCLK
J13	MGT_PROGCLK_3_PIN_P	GTY_REFCLKP0_203	MGT REFCLK
G12	MGT_PROGCLK_4_PIN_N	GTY_REFCLKN0_204	MGT REFCLK
G13	MGT_PROGCLK_4_PIN_P	GTY_REFCLKP0_204	MGT REFCLK
E12	MGT_PROGCLK_5_PIN_N	GTY_REFCLKN0_205	MGT REFCLK
E13	MGT_PROGCLK_5_PIN_P	GTY_REFCLKP0_205	MGT REFCLK
B14	MGT_PROGCLK_7_PIN_N	GTY_REFCLKN1_206	MGT REFCLK
B15	MGT_PROGCLK_7_PIN_P	GTY_REFCLKP1_206	MGT REFCLK
R40	PCIE_LCL_REFCLK_PIN_N	GTY_REFCLKN0_104	MGT REFCLK

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
R39	PCIE_LCL_REFCLK_PIN_P	GTY_REFCLKP0_104	MGT REFCLK
W40	PCIE_REFCLK_0_PIN_N	GTY_REFCLKN0_103	MGT REFCLK
W39	PCIE_REFCLK_0_PIN_P	GTY_REFCLKP0_103	MGT REFCLK
L40	PCIE_REFCLK_1_PIN_N	GTY_REFCLKN0_105	MGT REFCLK
L39	PCIE_REFCLK_1_PIN_P	GTY_REFCLKP0_105	MGT REFCLK
F19*	PCIE_RST_1V8_L (Rev4+)	PMC_MIO39_501	1.8
D19	PCIE_RST_1V8_L	PMC_MIO38_501	1.8
C45*	PCIE_RX0_N (Rev3-) PCIE_RX15_N (Rev4+)	GTY_RXN3_106	MGT
C44*	PCIE_RX0_P (Rev3-) PCIE_RX15_P (Rev4+)	GTY_RXP3_106	MGT
D47*	PCIE_RX1_N (Rev3-) PCIE_RX14_N (Rev4+)	GTY_RXN2_106	MGT
D46*	PCIE_RX1_P (Rev3-) PCIE_RX14_N (Rev4+)	GTY_RXP2_106	MGT
T47*	PCIE_RX10_N (Rev3-) PCIE_RX5_N (Rev4+)	GTY_RXN1_104	MGT
T46*	PCIE_RX10_P (Rev3-) PCIE_RX5_P (Rev4+)	GTY_RXP1_104	MGT
V47*	PCIE_RX11_N (Rev3-) PCIE_RX4_N (Rev4+)	GTY_RXN0_104	MGT
V46*	PCIE_RX11_P (Rev3-) PCIE_RX4_P (Rev4+)	GTY_RXP0_104	MGT
W45*	PCIE_RX12_N (Rev3-) PCIE_RX3_N (Rev4+)	GTY_RXN3_103	MGT
W44*	PCIE_RX12_P (Rev3-) PCIE_RX3_P (Rev4+)	GTY_RXP3_103	MGT
Y47*	PCIE_RX13_N (Rev3-) PCIE_RX2_N (Rev4+)	GTY_RXN2_103	MGT
Y46*	PCIE_RX13_P (Rev3-) PCIE_RX2_P (Rev4+)	GTY_RXP2_103	MGT
AA45*	PCIE_RX14_N (Rev3-) PCIE_RX1_N (Rev4+)	GTY_RXN1_103	MGT
AA44*	PCIE_RX14_P (Rev3-) PCIE_RX1_P (Rev4+)	GTY_RXP1_103	MGT
AB47*	PCIE_RX15_N (Rev3-) PCIE_RX0_N (Rev4+)	GTY_RXN0_103	MGT
AB46*	PCIE_RX15_P (Rev3-) PCIE_RX0_P (Rev4+)	GTY_RXP0_103	MGT

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
E45*	PCIE_RX2_N (Rev3-) PCIE_RX13_N (Rev4+)	GTY_RXN1_106	MGT
E44*	PCIE_RX2_P (Rev3-) PCIE_RX13_P (Rev4+)	GTY_RXP1_106	MGT
F47*	PCIE_RX3_N (Rev3-) PCIE_RX12_N (Rev4+)	GTY_RXN0_106	MGT
F46*	PCIE_RX3_P (Rev3-) PCIE_RX12_P (Rev4+)	GTY_RXP0_106	MGT
H47*	PCIE_RX4_N (Rev3-) PCIE_RX11_N (Rev4+)	GTY_RXN3_105	MGT
H46*	PCIE_RX4_P (Rev3-) PCIE_RX11_P (Rev4+)	GTY_RXP3_105	MGT
K47*	PCIE_RX5_N (Rev3-) PCIE_RX10_N (Rev4+)	GTY_RXN2_105	MGT
K46*	PCIE_RX5_P (Rev3-) PCIE_RX10_P (Rev4+)	GTY_RXP2_105	MGT
L45*	PCIE_RX6_N (Rev3-) PCIE_RX9_N (Rev4+)	GTY_RXN1_105	MGT
L44*	PCIE_RX6_P (Rev3-) PCIE_RX9_P (Rev4+)	GTY_RXP1_105	MGT
M47*	PCIE_RX7_N (Rev3-) PCIE_RX8_N (Rev4+)	GTY_RXN0_105	MGT
M46*	PCIE_RX7_P (Rev3-) PCIE_RX8_P (Rev4+)	GTY_RXP0_105	MGT
N45*	PCIE_RX8_N (Rev3-) PCIE_RX7_N (Rev4+)	GTY_RXN3_104	MGT
N44*	PCIE_RX8_P (Rev3-) PCIE_RX7_P (Rev4+)	GTY_RXP3_104	MGT
P47*	PCIE_RX9_N (Rev3-) PCIE_RX6_N (Rev4+)	GTY_RXN2_104	MGT
P46*	PCIE_RX9_P (Rev3-) PCIE_RX6_P (Rev4+)	GTY_RXP2_104	MGT
A44*	PCIE_TX0_PIN_N (Rev3-) PCIE_TX15_PIN_N (Rev4+)	GTY_TXN3_106	MGT
A43*	PCIE_TX0_PIN_P (Rev3-) PCIE_TX15_PIN_P (Rev4+)	GTY_TXP3_106	MGT
B42*	PCIE_TX1_PIN_N (Rev3-) PCIE_TX14_PIN_N (Rev4+)	GTY_TXN2_106	MGT
B41*	PCIE_TX1_PIN_P (Rev3-) PCIE_TX14_PIN_P (Rev4+)	GTY_TXP2_106	MGT

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
R44*	PCIE_TX10_PIN_N (Rev3-) PCIE_TX5_PIN_N (Rev4+)	GTY_TXN1_104	MGT
R43*	PCIE_TX10_PIN_P (Rev3-) PCIE_TX5_PIN_P (Rev4+)	GTY_TXP1_104	MGT
T42*	PCIE_TX11_PIN_N (Rev3-) PCIE_TX4_PIN_N (Rev4+)	GTY_TXN0_104	MGT
T41*	PCIE_TX11_PIN_P (Rev3-) PCIE_TX4_PIN_P (Rev4+)	GTY_TXP0_104	MGT
U44*	PCIE_TX12_PIN_N (Rev3-) PCIE_TX3_PIN_N (Rev4+)	GTY_TXN3_103	MGT
U43*	PCIE_TX12_PIN_P (Rev3-) PCIE_TX3_PIN_P (Rev4+)	GTY_TXP3_103	MGT
V42*	PCIE_TX13_PIN_N (Rev3-) PCIE_TX2_PIN_N (Rev4+)	GTY_TXN2_103	MGT
V41*	PCIE_TX13_PIN_P (Rev3-) PCIE_TX2_PIN_P (Rev4+)	GTY_TXP2_103	MGT
Y42*	PCIE_TX14_PIN_N (Rev3-) PCIE_TX1_PIN_N (Rev4+)	GTY_TXN1_103	MGT
Y41*	PCIE_TX14_PIN_P (Rev3-) PCIE_TX1_PIN_P (Rev4+)	GTY_TXP1_103	MGT
AB42*	PCIE_TX15_PIN_N (Rev3-) PCIE_TX0_PIN_N (Rev4+)	GTY_TXN0_103	MGT
AB41*	PCIE_TX15_PIN_P (Rev3-) PCIE_TX0_PIN_P (Rev4+)	GTY_TXP0_103	MGT
D42*	PCIE_TX2_PIN_N (Rev3-) PCIE_TX13_PIN_N (Rev4+)	GTY_TXN1_106	MGT
D41*	PCIE_TX2_PIN_P (Rev3-) PCIE_TX13_PIN_P (Rev4+)	GTY_TXP1_106	MGT
F42*	PCIE_TX3_PIN_N (Rev3-) PCIE_TX12_PIN_N (Rev4+)	GTY_TXN0_106	MGT
F41*	PCIE_TX3_PIN_P (Rev3-) PCIE_TX12_PIN_P (Rev4+)	GTY_TXP0_106	MGT
G44*	PCIE_TX4_PIN_N (Rev3-) PCIE_TX11_PIN_N (Rev4+)	GTY_TXN3_105	MGT
G43*	PCIE_TX4_PIN_P (Rev3-) PCIE_TX11_PIN_P (Rev4+)	GTY_TXP3_105	MGT
H42*	PCIE_TX5_PIN_N (Rev3-) PCIE_TX10_PIN_N (Rev4+)	GTY_TXN2_105	MGT
H41*	PCIE_TX5_PIN_P (Rev3-) PCIE_TX10_PIN_P (Rev4+)	GTY_TXP2_105	MGT

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
J44*	PCIE_TX6_PIN_N (Rev3-) PCIE_TX9_PIN_N (Rev4+)	GTY_TXN1_105	MGT
J43*	PCIE_TX6_PIN_P (Rev3-) PCIE_TX9_PIN_P (Rev4+)	GTY_TXP1_105	MGT
K42*	PCIE_TX7_PIN_N (Rev3-) PCIE_TX8_PIN_N (Rev4+)	GTY_TXN0_105	MGT
K41*	PCIE_TX7_PIN_P (Rev3-) PCIE_TX8_PIN_P (Rev4+)	GTY_TXP0_105	MGT
M42*	PCIE_TX8_PIN_N (Rev3-) PCIE_TX7_PIN_N (Rev4+)	GTY_TXN3_104	MGT
M41*	PCIE_TX8_PIN_P (Rev3-) PCIE_TX7_PIN_P (Rev4+)	GTY_TXP3_104	MGT
P42*	PCIE_TX9_PIN_N (Rev3-) PCIE_TX6_PIN_N (Rev4+)	GTY_TXN2_104	MGT
P41*	PCIE_TX9_PIN_P (Rev3-) PCIE_TX6_PIN_P (Rev4+)	GTY_TXP2_104	MGT
M37	PERST_PL_L	IO_L0P_306	1.8
J34	PL_SCL	IO_L9P_306	1.8
J35	PL_SDA	IO_L9N_306	1.8
F17	PMC_I2C_SCL	PMC_MIO50_501	1.8
G17	PMC_I2C_SDA	PMC_MIO51_501	1.8
L19	PMOD_IO1	IO_L2N_406	3.3
L18	PMOD_IO2	IO_L3P_406	3.3
K17	PMOD_IO3	IO_L3N_406	3.3
L20	PMOD_IO4	IO_L4P_406	3.3
K21	PMOD_IO5	IO_L4N_406	3.3
K18	PMOD_IO6	IO_L5P_HDGC_406	3.3
J18	PMOD_IO7	IO_L5N_406	3.3
K20	PMOD_IO8	IO_L6P_HDGC_406	3.3
F34	QSPI0_CLK_PIN	PMC_MIO0_500	1.8
F32	QSPI0_CS_B	PMC_MIO5_500	1.8
E33	QSPI0_IO[0]	PMC_MIO4_500	1.8
G34	QSPI0_IO[1]	PMC_MIO1_500	1.8
H33	QSPI0_IO[2]	PMC_MIO2_500	1.8
F33	QSPI0_IO[3]	PMC_MIO3_500	1.8
N31	QSPI1_CLK_PIN	PMC_MIO12_500	1.8
H32	QSPI1_CS_B	PMC_MIO7_500	1.8
K32	QSPI1_IO[0]	PMC_MIO8_500	1.8

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
L32	QSPI1_IO[1]	PMC_MIO9_500	1.8
M32	QSPI1_IO[2]	PMC_MIO10_500	1.8
N32	QSPI1_IO[3]	PMC_MIO11_500	1.8
B21	SDIO_1V8_CLK_PIN	PMC_MIO26_501	1.8
E21	SDIO_1V8_CMD	PMC_MIO29_501	1.8
F20	SDIO_1V8_DAT0	PMC_MIO30_501	1.8
E20	SDIO_1V8_DAT1	PMC_MIO31_501	1.8
D20	SDIO_1V8_DAT2	PMC_MIO32_501	1.8
B20	SDIO_1V8_DAT3	PMC_MIO33_501	1.8
D21	SDIO_1V8_DETECT	PMC_MIO28_501	1.8
A20	SDIO_1V8_SEL	PMC_MIO34_501	1.8
AW2	SI5328_0_RST_1V5_L	IO_L1P_N0P2_M3P56_710	1.5
AW3	SI5328_1V5_C2B	IO_L2P_N0P4_M3P58_710	1.5
AV2	SI5328_1V5_INT_C1B	IO_L1N_N0P3_M3P57_710	1.5
AU3	SI5328_1V5_LOL	IO_L3N_XCC_N1P1_M3P61_710	1.5
AV3*	SI5328_1V5_RATE0 (Rev3-)	IO_L2N_N0P5_M3P59_710	1.5
AT3*	SI5328_1V5_RATE1 (Rev3-)	IO_L3P_XCC_N1P0_M3P60_710	1.5
AT1	SI5328_1V5_SCL	IO_L0N_XCC_N0P1_M3P55_710	1.5
AT2	SI5328_1V5_SDA	IO_L0P_XCC_N0P0_M3P54_710	1.5
M14	SI5328_OUT_0_PIN_N	GTY_REFCLKN1_201	MGT REFCLK
M15	SI5328_OUT_0_PIN_P	GTY_REFCLKP1_201	MGT REFCLK
F14	SI5328_OUT_1_PIN_N	GTY_REFCLKN1_204	MGT REFCLK
F15	SI5328_OUT_1_PIN_P	GTY_REFCLKP1_204	MGT REFCLK
AD10	SI5328_REFCLK_IN_N	GTY_REFCLKN1_200	MGT REFCLK
AD11	SI5328_REFCLK_IN_P	GTY_REFCLKP1_200	MGT REFCLK
AM3*	SI5328_REFCLK_IN2_N (Rev4+)	IO_L6N_GC_XCC_N2P1_M3P67_710	1.5
AN3*	SI5328_REFCLK_IN2_P (Rev4+)	IO_L6P_GC_XCC_N2P0_M3P66_710	1.5
K33	SPARE_SCL	IO_L3N_306	1.8
K37	SPARE_SDA	IO_L4P_306	1.8
J36	SPARE_WP	IO_L4N_306	1.8
H19	SRVC_MD_L	IO_L9P_406	3.3
E18	UART0_RXD	PMC_MIO42_501	1.8
D18	UART0_TXD	PMC_MIO43_501	1.8
B17	UART1_RXD	PMC_MIO47_501	1.8
A17	UART1_TXD	PMC_MIO46_501	1.8
F30	USB_ULPI_CLK	PMC_MIO18_500	1.8

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage
K31	USB_ULPI_DATA[0]	PMC_MIO14_500	1.8
J31	USB_ULPI_DATA[1]	PMC_MIO15_500	1.8
H31	USB_ULPI_DATA[2]	PMC_MIO16_500	1.8
G31	USB_ULPI_DATA[3]	PMC_MIO17_500	1.8
G30	USB_ULPI_DATA[4]	PMC_MIO19_500	1.8
J30	USB_ULPI_DATA[5]	PMC_MIO20_500	1.8
K30	USB_ULPI_DATA[6]	PMC_MIO21_500	1.8
L30	USB_ULPI_DATA[7]	PMC_MIO22_500	1.8
M30	USB_ULPI_DIR	PMC_MIO23_500	1.8
L29	USB_ULPI_NXT	PMC_MIO25_500	1.8
M31	USB_ULPI_RST	PMC_MIO13_500	1.8
M29	USB_ULPI_STP	PMC_MIO24_500	1.8
M20	USER_LED_G0_1V8	IO_L0P_406	3.3
M21	USER_LED_G1_1V8	IO_L0N_406	3.3
G36	USR_SW_0	IO_L10P_306	1.8
G37	USR_SW_1	IO_L10N_306	1.8

Table 12 : Complete Pinout Table

Note:
* Signals that have changed at rev4 (SN157 and newer, delivered in 2023 and later)

Revision History

Date	Revision	Changed By	Nature of Change
23 July 2021	0.1	K. Roth	Draft.
30 August 2021	1.0	C. Gutierrez	adding uSD/QSPI boot sections.
13 December 2021	1.1	K. Roth	Changed reference of PCIe Gen4x16 to dual PCIe Gen4x8 throughout as per Xilinx product updates.
14 January 2022	1.2	K. Roth	Added example of changing boot modes to section Boot Modes.
31 May 2022	1.3	K. Roth	Added details about standalone operation in Power Requirements, added details about mechanical retention in Mechanical Requirements
28 Jul 2022	1.4	K. Roth	Corrected DDR4 density details in DDR4 SDRAM.
10 Oct 2022	1.5	K. Roth	Added figure FMC site access, added section Handling Instructions, Removed superfluous steps in Building and Programming uSD Configuration Images, added section Battery
11 Nov 2022	2.0	K. Roth	Added support for rev4 PCBs: Updated appendix MIO Map with second PCIe reset, updated appendix Complete Pinout Table with second PCIe reset and pcie lane inversion, modified PCI Express to add box noting the PCIE lane inversion at rev4, added Clock Topology Rev4+ (SN157 and newer), modified Clocking to include LMK61E2, modified Si5328 to detail CLKNIN2 ACAP PL connection on rev4+, modified GEM0 to include rev4+ PHY Microchip VSC8541 and LED connections, added LMK61E2 and Si5338, added links to UART and JTAG within Micro USB Interface
12 Jul 2023	2.1	K. Roth	Updated section Thermal Performance with installed fan thermal performance, split tables in Physical Specifications for clarity, added DDR4 slew constraints to DDR4 SDRAM, corrected fully assembled weight.
31 Dec 2024	2.2	K. Roth	Corrected syntax error in pinout table and switch index mistake.

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